



ASIC's for HEP Tracking and Vertexing: radiation, scaling, power, cost

**key technological limitations to address
the P5 science drivers**

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Contents



- IC Design in US HEP report from 2013
- (aka is there any point to this talk...?)
- Challenges, Baseline Solutions, more Adventurous Solutions
- Challenge-by-challenge commentary / examples
- 2013 Report recommendations



White Paper:

Integrated Circuit Design in US High Energy Physics

July 10, 2013

- <http://arxiv.org/abs/1307.3241>
- Dedicated workshop May 30 – June 1, 2013
 - <https://indico.physics.lbl.gov/indico/conferenceDisplay.py?confId=2>
- Was a pre-meeting for Snowmass
- Report made recommendations (to ourselves)
- Fair to say that we have yet to seriously follow any of them
 - All still valid today
 - Will quote them as the conclusion to this talk



Challenges



- **Processes, Access, and Design**
 - **Is Cost a Challenge?**
 - **Literacy sharing design knowledge**
 - **Radiation Tolerance**
 - **Reliability**
 - **Power**
 - **Data Transmission**
 - **Functionality**
-



Baseline Solutions



- **Processes, Access, and Design**
 - CERN frame contracts (too soon to judge?)
- **Is Cost a Challenge?**
 - Collaboration
- **Literacy and sharing design knowledge**
 - Collaboration examples outside US
- **Radiation Tolerance**
 - Solved itself
- **Reliability**
 - Modest efforts to evaluate seriously. Have not suffered from it yet
- **Power**
 - Low sensor capacitance . Off-chip DC/DC. Serial power
- **Data Transmission**
 - Has escalated to a bigger challenge than it used to be
- **Functionality**
 - New processes, new designs



More Adventurous Solutions



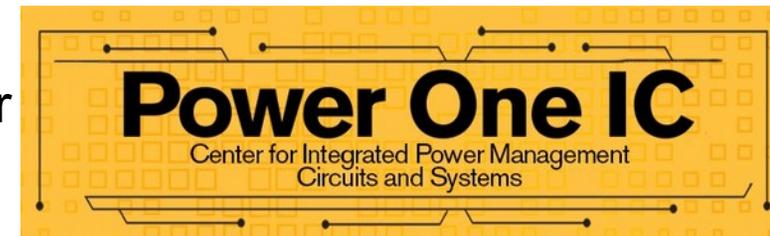
- **Processes, Access, and Design**
 - Look outside HEP (example)
- **Is Cost a Challenge?**
 - New technologies (examples)
- **Literacy and sharing design knowledge**
 - Have physics students take IC design / HDL courses. US IC collaboration?
- **Radiation Tolerance**
 - New regime beyond “solved itself” DSM tolerance
- **Reliability**
 - Needs more attention
- **Power**
 - Completely new technology? Join academic-industry partnerships?
- **Data Transmission**
 - Need help from outside HEP
- **Functionality**
 - Take advantage of Moore's Law



Process, Access, and Design (2)



- Can we engage vast EE IC design resources in the US?
- Example submitted by Mitch:
 - An excellent example of the potential for this kind of association is the interest expressed by Yun Chui at UT Dallas (<http://www.utdallas.edu/~chiu.yun/>) has been making an effort to find funding for a student to carry out the design of a SEU tolerant fast and low power ADC for the upgrade of LHC detectors.
- Several other ongoing efforts- all have a common problem: need to provide funding to pay EE students.
 - U. Washington, Seattle- digital design
 - UC Berkeley Wireless Research Center (drivers/receivers for *wired* high speed)
 - Recently formed Power One IC NSF center for academic-industry collaboration on IC power management design
 - Note, DOE can join this consortium- just have to
 - pay the \$50K membership fee like member companies do.



<https://poweroneic.asu.edu/join-power-one-ic/>



Is Cost A Challenge? (1)



- Mask cost was one of the big concerns for moving to 65nm CMOS
 - Let's look at upgrade construction costs, for example ATLAS pixels
 - Numbers in recently released “scoping document” (in a bit more detail than shown there)
 - Total pixel M&S cost: \$32M
 - Sensor cost: \$ 7M
 - Bump bonding cost \$ 9M
 - 65nm readout chip wafer cost \$ 2M
 - 65nm chip mask cost \$ 1M
 - (maybe instead of reducing readout chip cost, keep the chip and cut “everything else” => CMOS MAPS)
- What about prototyping cost?
 - 12mm² MPR in 65nm costs \$70K
 - 1 FTE expert designers costs 300-500K, and 1 FTE is not enough to make use of 12mm² in 65nm.



Is Cost A Challenge? (2)



- The real challenge is reducing design labor cost
 - Back to question of tapping into EE resources
 - 2nd component is for physics students to do IC design
 - After all, digital design is code, and we could not afford 10% of the data analysis code we use if we paid computing professionals to write it all
- Mask cost reduction may also be possible with new design technology
- 1D layout, as used for CMOS processes below 32nm, could be applied to larger features
 - 14nm (eg) features are NOT defined lithographically from patterns on masks (this is impossible using 192nm light)
 - They are defined by “pitch division” processing of regular patterns with larger features, printed lithographically
 - One can similarly make 65nm features using “cheap” 250nm masks, as long as one makes regular “1D layout” patterns



IC Design Literacy and sharing design knowledge



- Why do US physics students know C++, Python, etc. But not Verilog?
- Why can they use GEANT, but not SPICE?

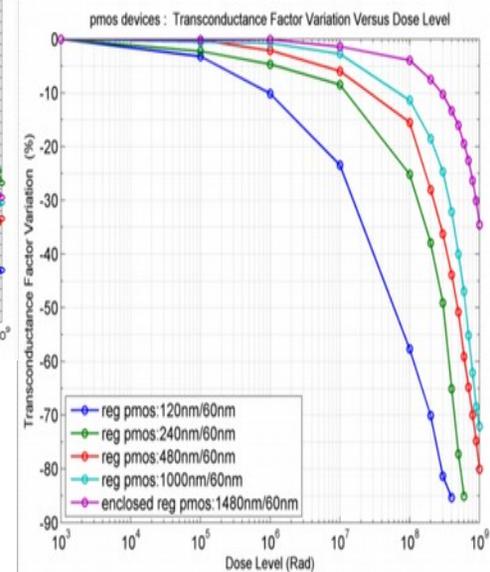
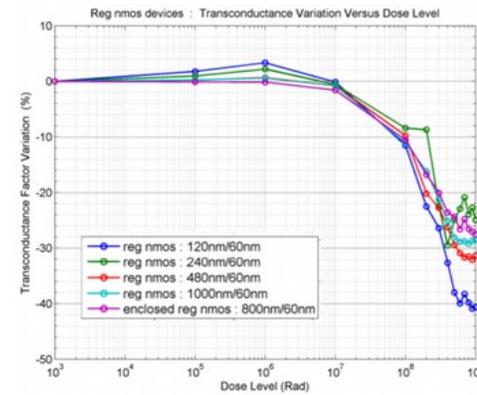
- Examples provided by Mitch of national HEP IC programs elsewhere
 - restrict what each institute does- manage program as a whole
 - Common knowledge-base and process choices. No need to reinvent the wheel every time
- strong national effort in France that has been quite productive and that CERN has a model that is very good at an international level, Germany has several very collaborative efforts



Radiation Tolerance (1)



- Sure, leaky gate oxide doesn't charge up
- But there is still STI
- Can't just design with small transistors
- (=dense logic) and expect nothing to
- happen after 100's of Mrads
- Need radiation corners. Need to design for radiation damage

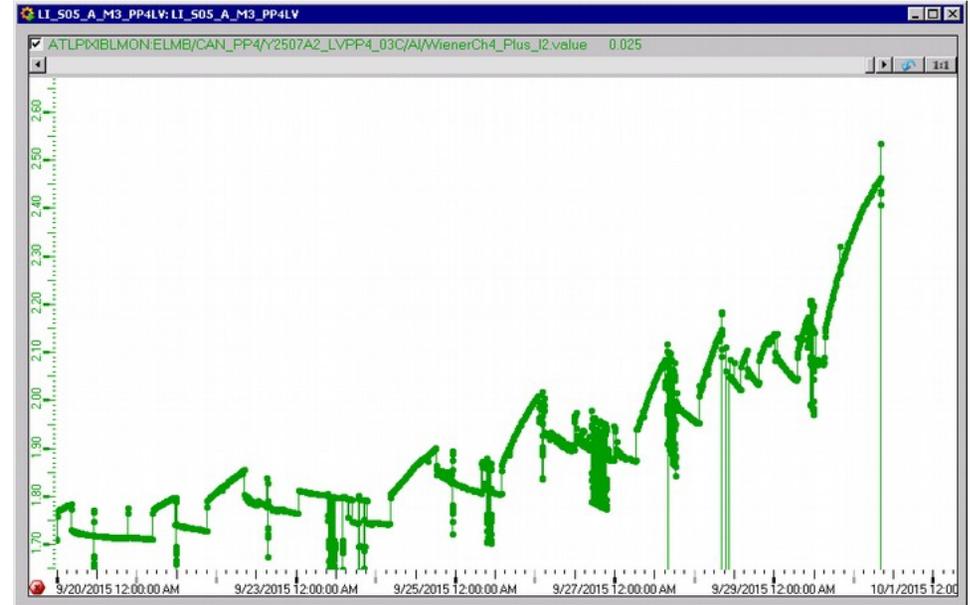


- And for HL-LHC we are now taking about running chips during fairly high dose irradiation.
 - Chips at the inner layer will get 300krad during a few hour run
 - this is the dose enough to kill the first rad-hard CDF SVX'
 - Radiation effects with short time constants will be important
 - They already are...

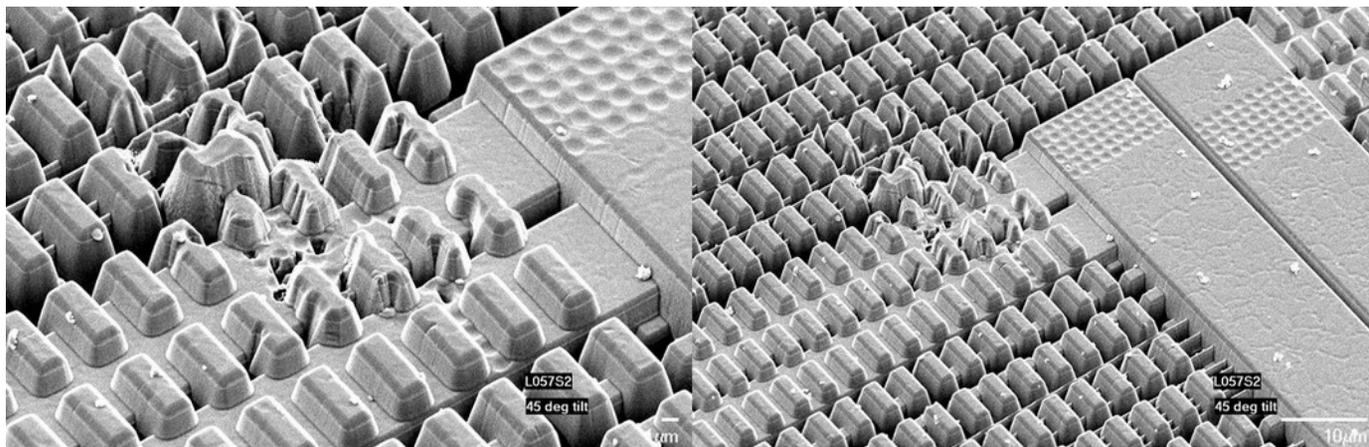


Radiation Tolerance (2)

- ATLAS IBL prompt effect not yet understood (130nm FE-I4 chip)
(disclaimer- could turn out to be something stupid and not a widely relevant radiation effect)



- STAR HFT catastrophic latchup
- Probably not relevant for pure bulk CMOS on low resistivity substrate, but thin chips and devices on high resistivity beware



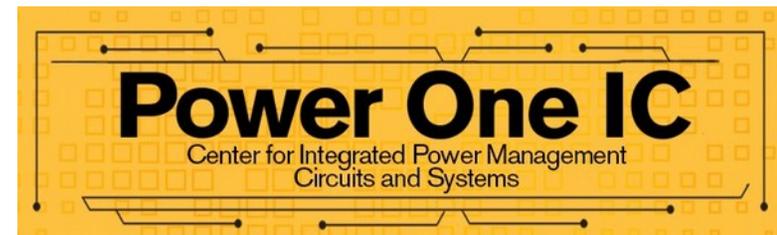


Power



- **Completely new technology (other than Si CMOS)?**
 - Large number of things put there
 - Range from modifications to CMOS to very exotic (will not list)
 - Irrelevant in short term- is there a long term benefit investing effort to look into them? Or let industry decide and then follow?
- **Academic/Industry partnerships**
 - HEP discrete DC-DC converter technology (eg FEAST) not very sophisticated
 - On-chip DC-DC very active in EE departments and industry

(repeated link:

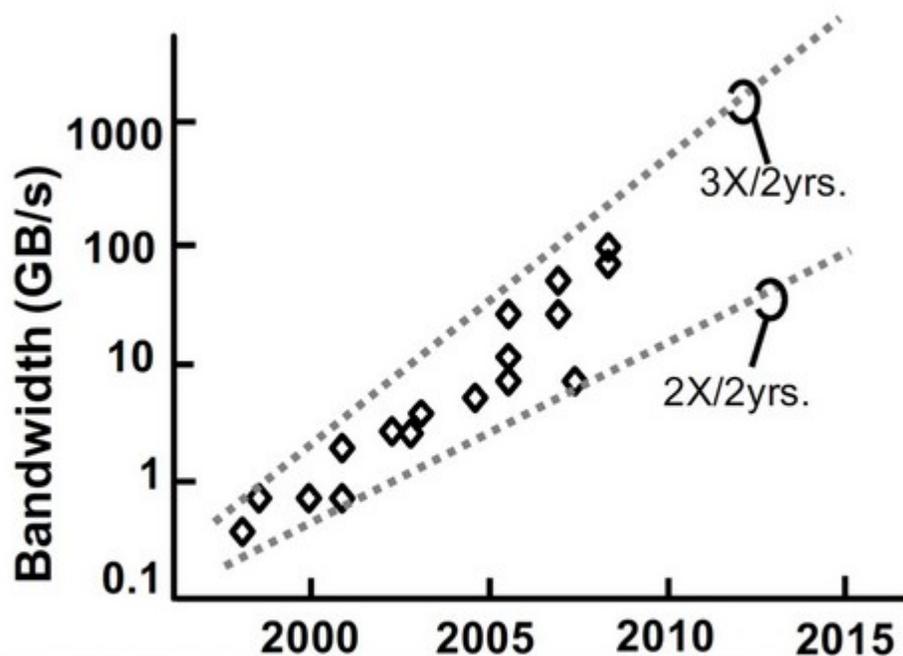


<https://poweroneic.asu.edu/join-power-one-ic/>



Data Transmission (1)

- Run 1 LHC experiments used chip output rates of order 100Mbps
 - 20x below commercial IC's in 2005
- Now aiming for 5-20Gbps per chip
 - Also 20x below commercial in 2015



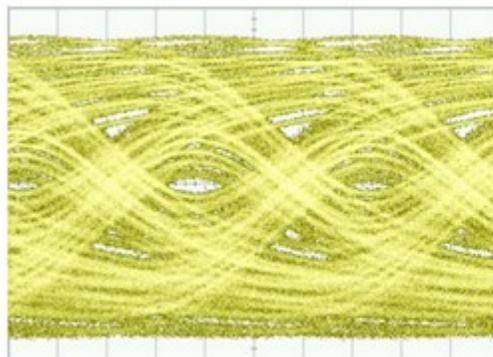
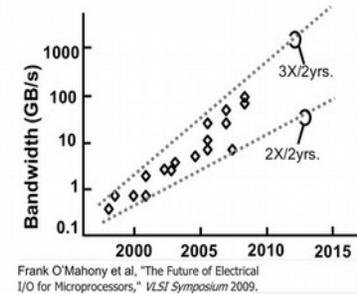
Frank O'Mahony et al, "The Future of Electrical I/O for Microprocessors," *VLSI Symposium* 2009.



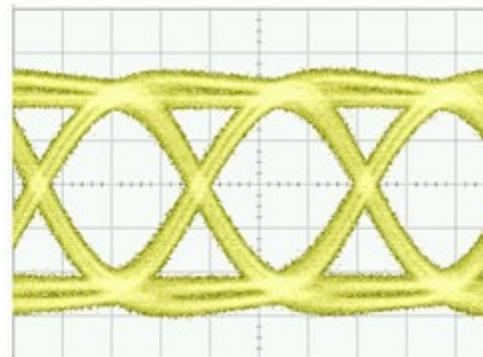
Functionality



- BUT, commercial chips drive short distances on PCBs
- HEP chips need to drive long distances on cables
- Factor of 20 is actually not that crazy comparing
- 1m to 5m distance
- BUT, at 100MHz signal distortion from cable was minor- ignored it
- At 5 Gbps distortion is huge!
 - Sophisticated equalization used in industry is needed!
(this is more than just a little pre-emphasis)
 - Very little experience within HEP. Help from EE departments needed.



15Gb/s Eye w/o Equalization

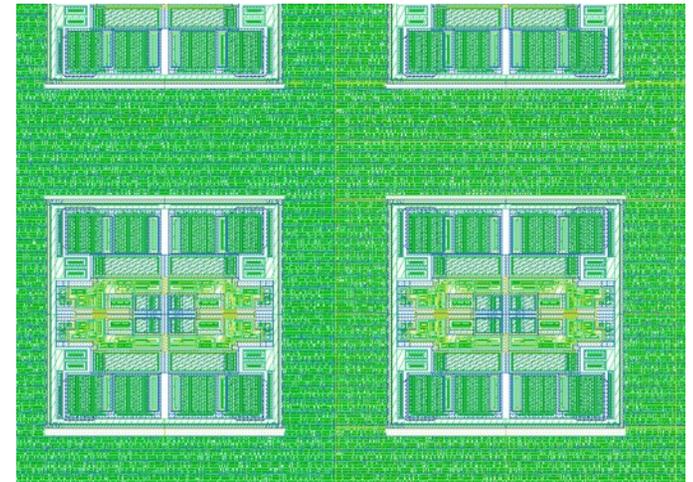


15Gb/s Eye after Equalization



Functionality

- High density logic and modern digital design tools make huge digital processing power available within a chip
- Just have to figure out what to do with it!
 - Shift in way we design chips to more digital
- MAPS- one chip does it all
- Wide range of processes to be understood
- New challenge for access and design
 - (Will always be hard to mix high logic density with MAPS)
- MAPS hybrids
 - 3D integration





IC Design in US HEP Recommendations



6.2 Recommendations

1. Continue to encourage the strong physicist-IC designer links in the US. This is a vital part of innovation and also important to the educational/training mission.
2. Seek to increase generic ASIC R&D to keep up with technology.
3. Basic literacy on IC technology should be included in the education of physics students to facilitate the communication between physicists and engineers, which is especially true for analog circuits for detectors.
4. To facilitate communication among designers, hold a yearly workshop of US IC designers. Include technical training to keep up with industry developments.
5. A point-of-contact for each institute should be identified to facilitate communication between groups and to follow up on recommendations in this report.
6. Investigate practical options for a designer at institute A to work a small fraction of time on a project at institute B on which institute A is not involved. This would be very helpful for load balancing in small groups- particularly universities.
7. Complete and maintain an up-to-date catalog of existing ASICs as shown in the appendix 6.4.
8. Consider a scientific ASIC design stewardship role for HEP, analogous to the particle accelerator stewardship role.



BACKUP



Rad Hard logic lagged Moore's Law due to ELT, but now caught up

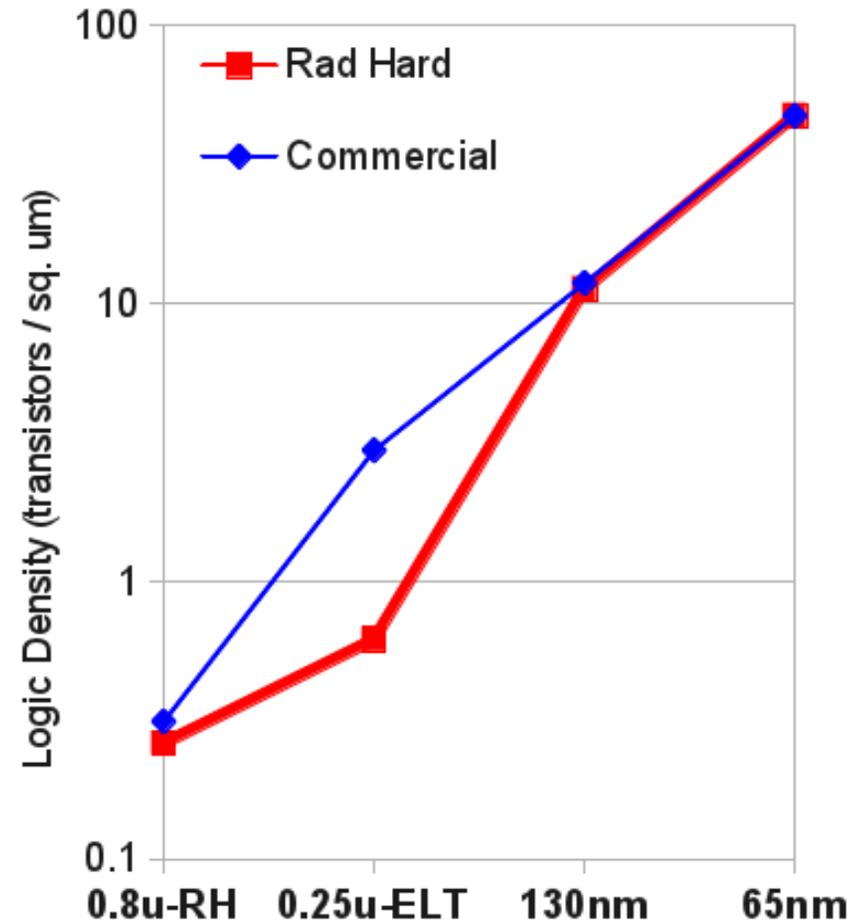
65nm



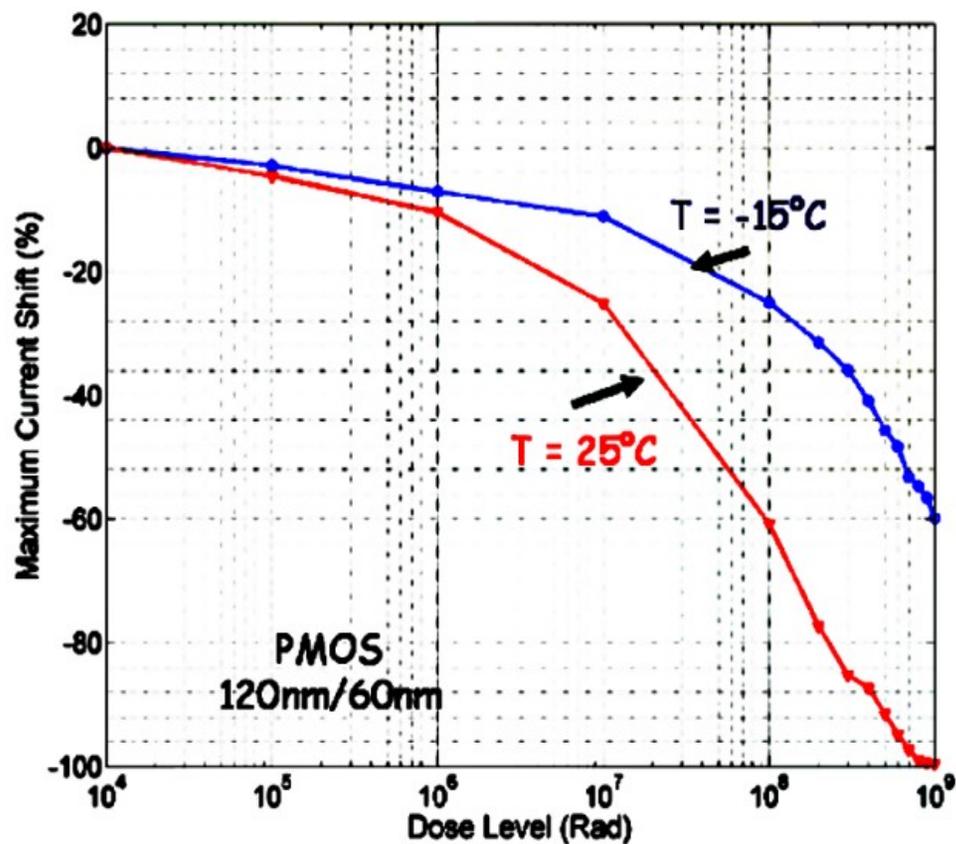
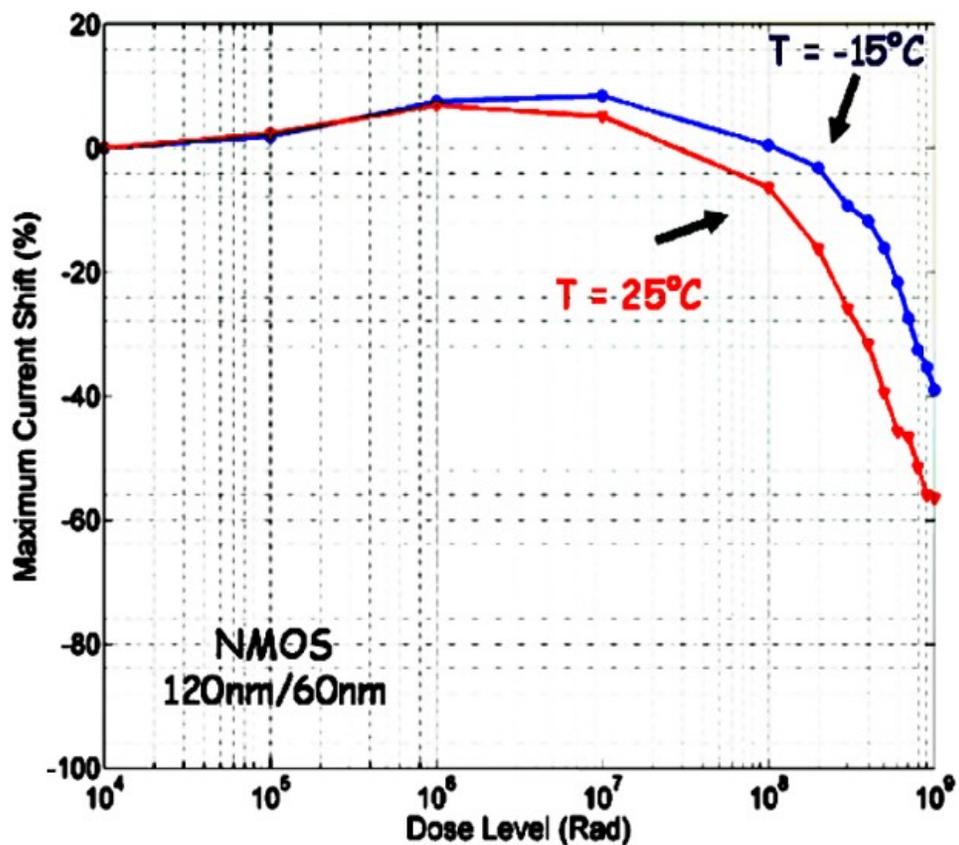
130nm



0.25um
ELT



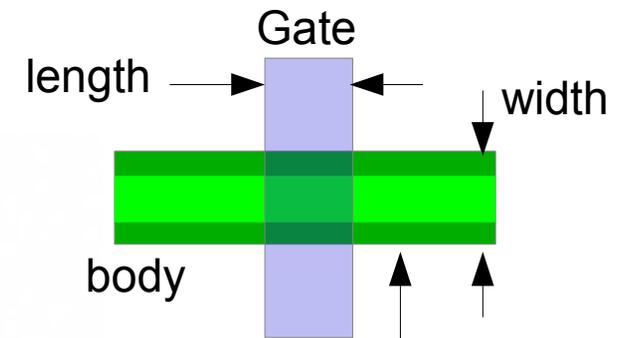
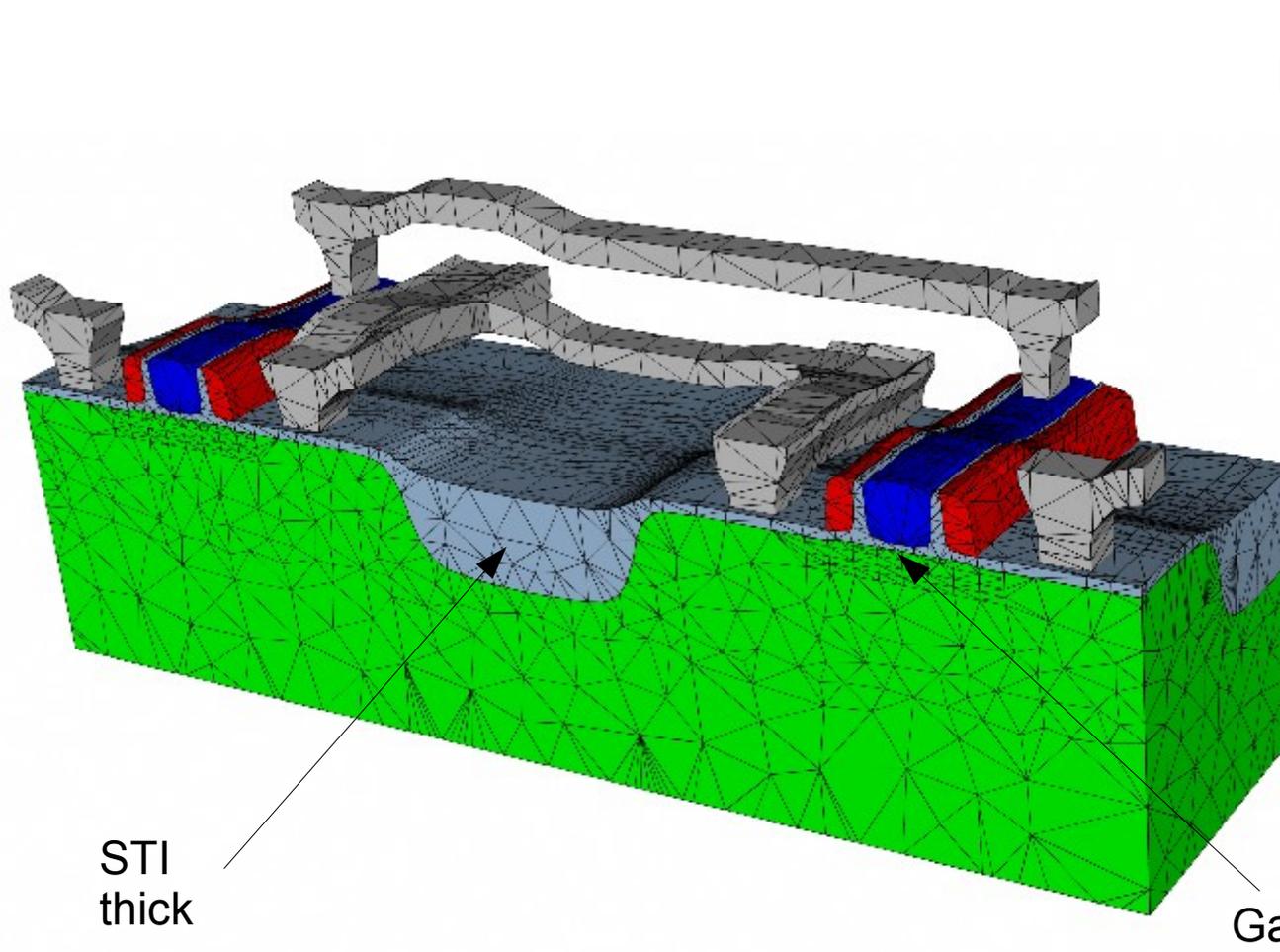
Minimum size at different temperature





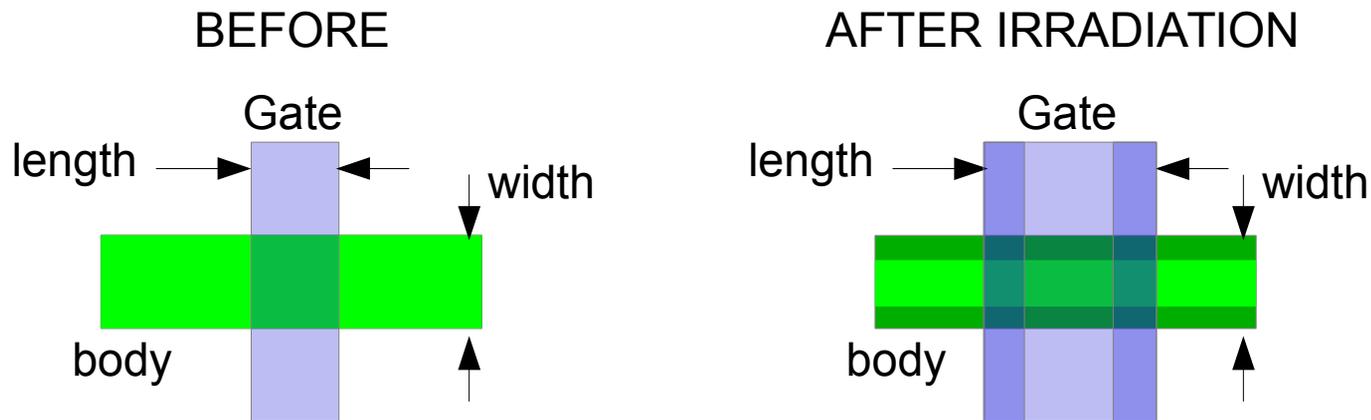
Effect of STI charge buildup (RINCE)

F.Faccio and G.Cervelli, IEEE TRANS. NUCL. SCI, VOL. 52, NO. 6, 2005



As body get narrower and narrower charge trapped in STI acts as "side gates" to the channel (a parasitic finfet)
NMOS opens up, PMOS pinches off.

+ A previously unobserved length effect



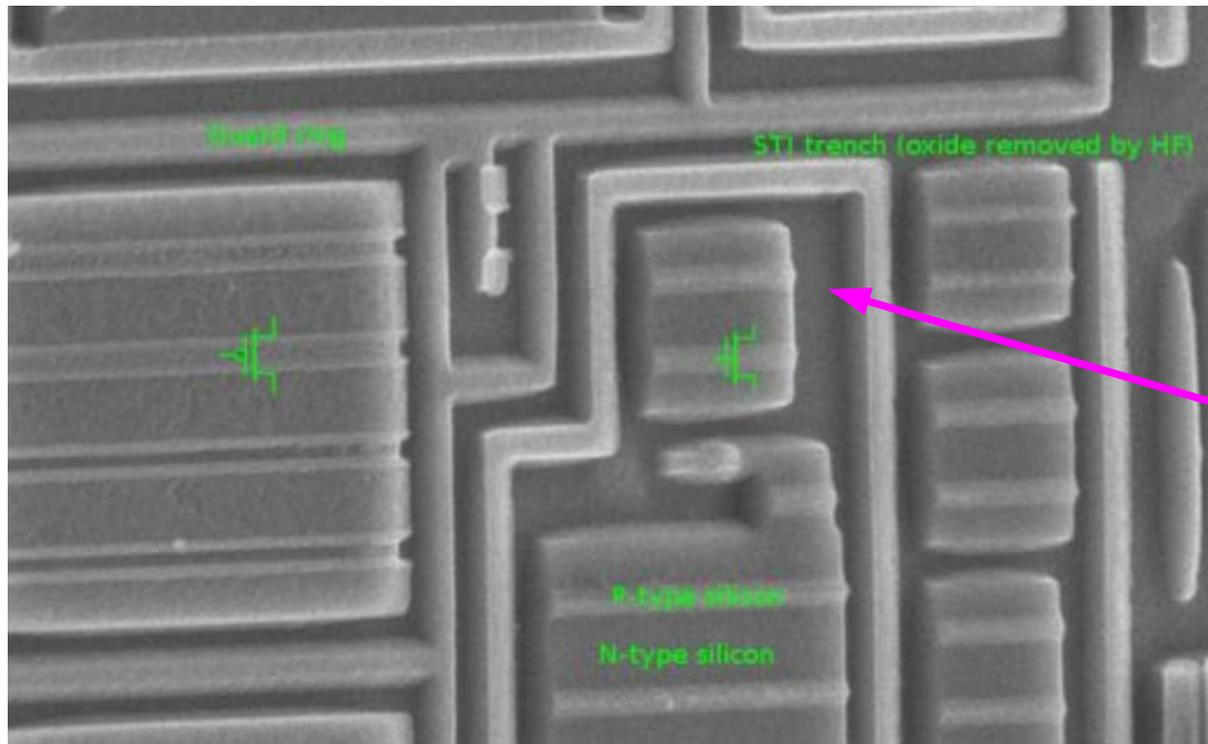
Obviously not a physical lengthening of the channel
Behaves as if this happens

- Length mechanism characterized empirically but device physics not understood
- Both small width and small length get hit- not good news for min. Size devices.
- (Same effects are there in 130nm, but can't make small enough transistors to clearly see them)



Width effect has a known damage mechanism

- **Small feature size CMOS technology is radiation hard because the gate oxide is leaky due to QM tunneling. This prevents charge build-up in the gate oxide**
- **But there are other oxides that are not thin enough for QM tunneling, and charge trapping in them eventually matters.**



These trenches are normally full of oxide called STI (shallow trench isolation)



RD53



www.cern.ch/RD53



RD-53 Collaboration Home



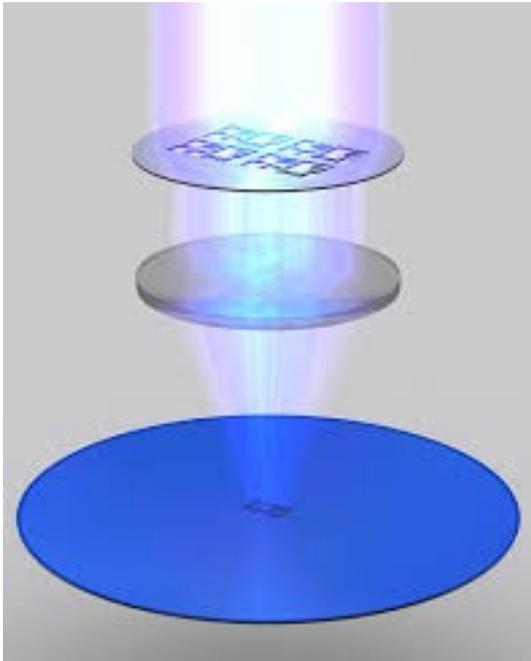
RD-53 will develop the tools and designs needed to produce the next generation of pixel readout chips needed by [ATLAS](#) and [CMS](#) at the [HL-LHC](#). There is also interest and participation by [CLIC](#). More details can be found in the [collaboration proposal](#).

* [Meetings](#) * [Documents](#) (including papers) * [Press](#) * [Conferences](#) *





Familiar photo-lithography



Photoresist pattern is a copy of the mask pattern



That's not how it works any more



- **Feature size in many of your pockets is 20nm**
- **Phones with 14nm chips are being sold this year**
- **10nm is just around the corner**

but all these were / will be fabricated with 193nm wavelength light !

- **Immersion lithography can get you as far as $\lambda/6$**



Can make arbitrarily fine parallel lines with processing

193 nm light is just the first step

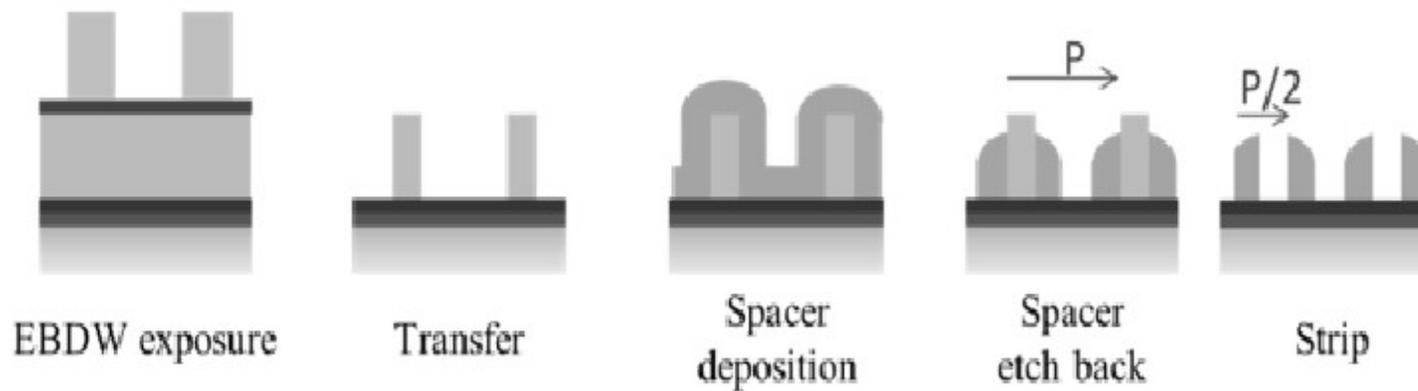


Fig.1: Pitch division process sequence from left to right.



Lines and cuts fabrication

- **Transistors are NOT a copy of any mask**
- **They are formed by cutting parallel lines**
- **Cuts are made by a laser or e-beam shining through orthogonal parallel lines**

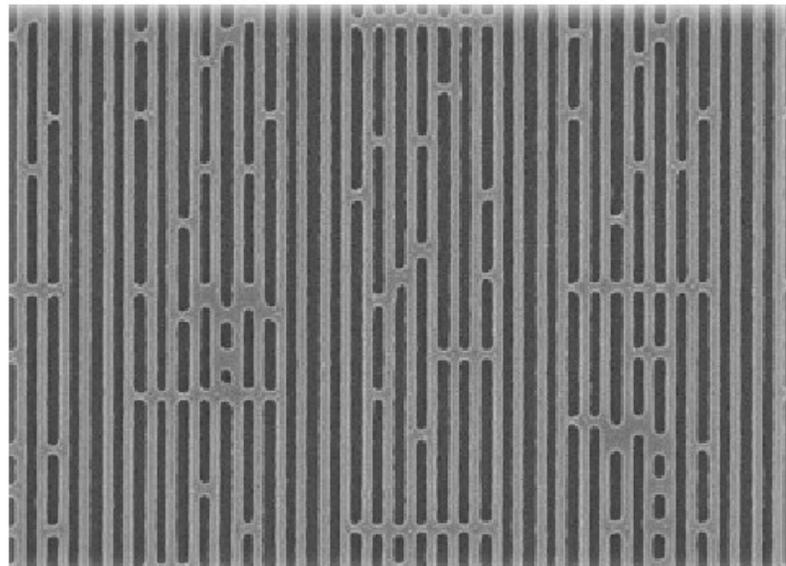


Fig 2: SEM image of typical "lines and cuts" pattern with 20nm feature size