

# BNL Readout & Trigger/DAQ Roadmap

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# Outline

- Introduction
  - R&D of Integrated Solutions for Readout & Trigger/DAQ Systems
- Readout and Trigger/DAQ at BNL
  - Hadron Collider Experiment: ATLAS Detector Upgrade
  - Noble Liquid TPCs for Neutrino Experiments:  
Low Noise Multiplexed Readout integrated on the TPC electrodes
- Conclusion

# Introduction (1)

- R&D at BNL has been focused on the overall *readout* system optimization for experiments
  - Initiated by physics motivation, start from detector & readout development, to trigger and DAQ implementation
  - *Not trying to develop one solution fits all*
  - Great leverage of expertise available in Physics Department and Instrumentation Division, covering various areas, from detector, readout to trigger and DAQ
- *Goals of R&D: Continuously develop expertise in select sensor and electronics technologies, aimed to efficiently provide integrated solutions of Readout and Trigger/DAQ systems optimized for some key future experiments*

# Introduction (2)

- The Readout and Trigger/DAQ development at BNL has been following this trend and focused on the following two areas
  - *Operation in radiation environment at high collider luminosity*
  - *Operation in noble liquids (e.g. LAr at ~89K)*
- Front end ASICs and board design are being *optimized for two distinctly different sets* of experimental and environmental conditions
  - *High counting rates, magnetic field and radiation for LHC*
  - *Cryogenic temperature, waveform recording* at low rates, for noble liquid TPCs
- Trigger/DAQ design explores the use of COTS solution (high speed optical links, DSP in FPGA etc.), where possible
- *P5 recommendation 27: Focus resources toward directed instrumentation R&D in the near-term for high-priority projects. As the technical challenges of current high-priority projects are met, restore to the extent possible a balanced mix of short-term and long-term R&D*

# Introduction (3)

- **Energy Frontier** Experiments
  - ATLAS Phase-I Upgrade
  - ATLAS Phase-II Upgrade
- **Intensity Frontier** Experiments
  - MicroBooNE
  - SBND
  - DUNE Far Detector

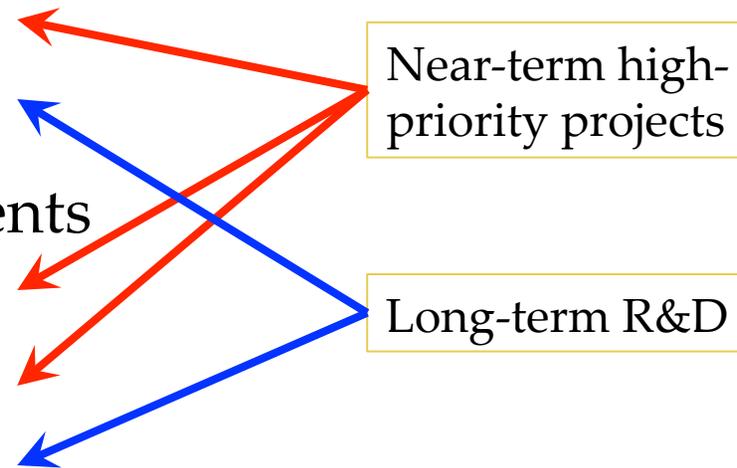
# Introduction (3)

- Energy Frontier Experiments

- ATLAS Phase-I Upgrade
- ATLAS Phase-II Upgrade

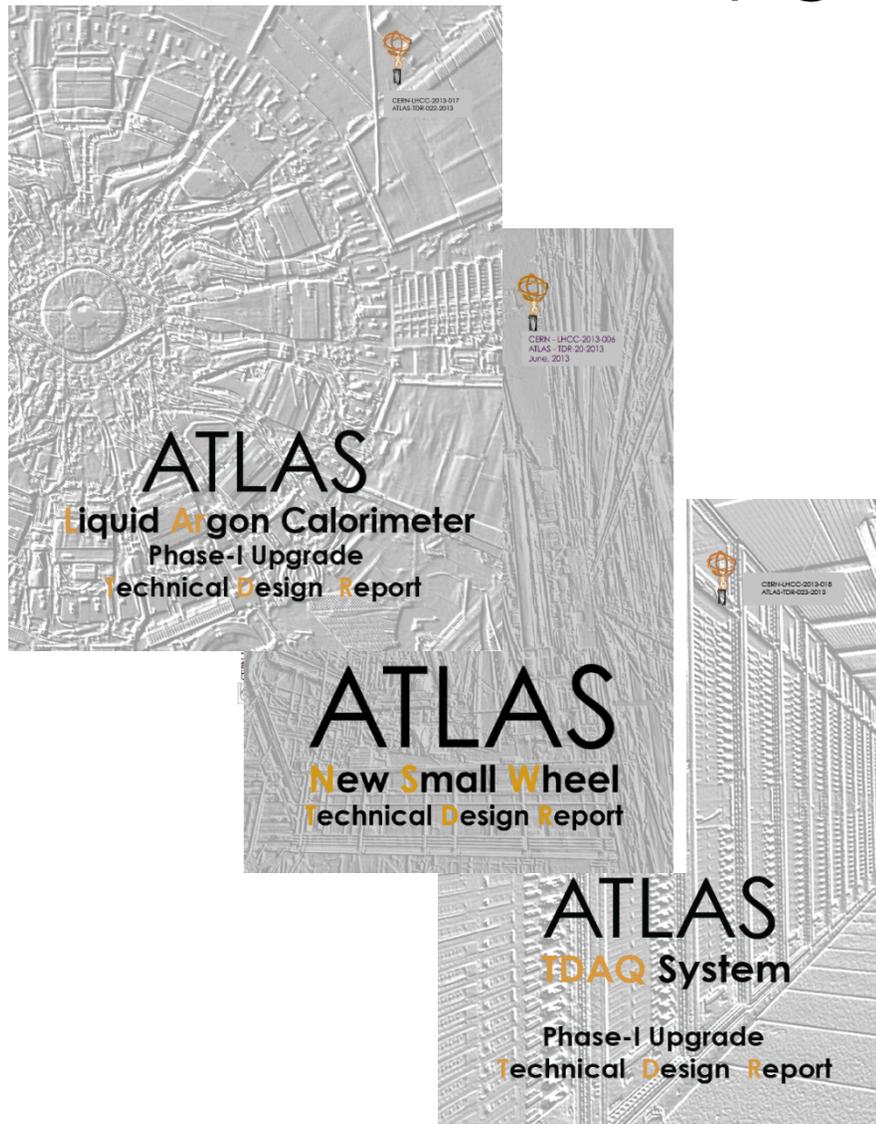
- Intensity Frontier Experiments

- MicroBooNE
- SBND
- DUNE Far Detector



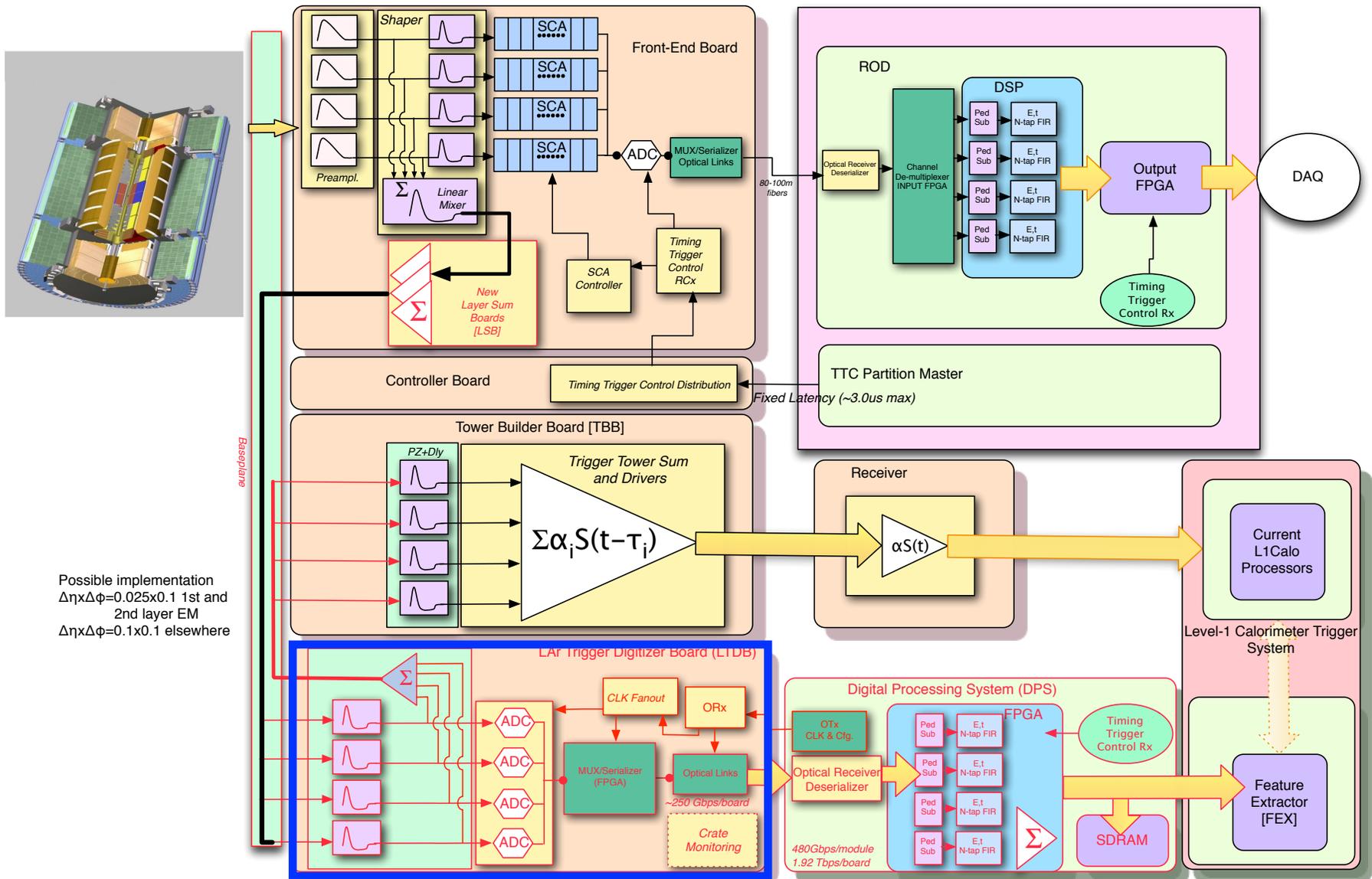
# Hadron Collider Experiment: ATLAS Detector Upgrade

# ATLAS Phase-I Upgrade



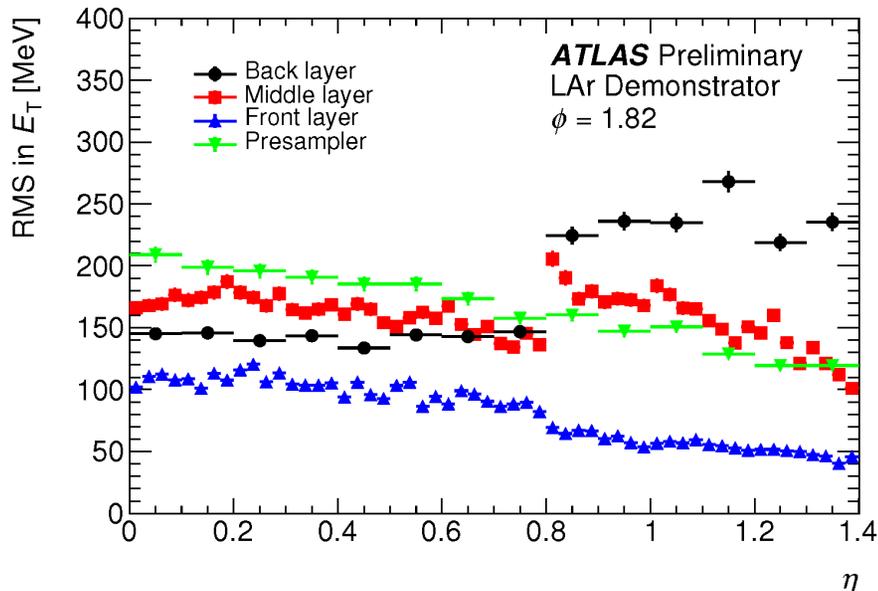
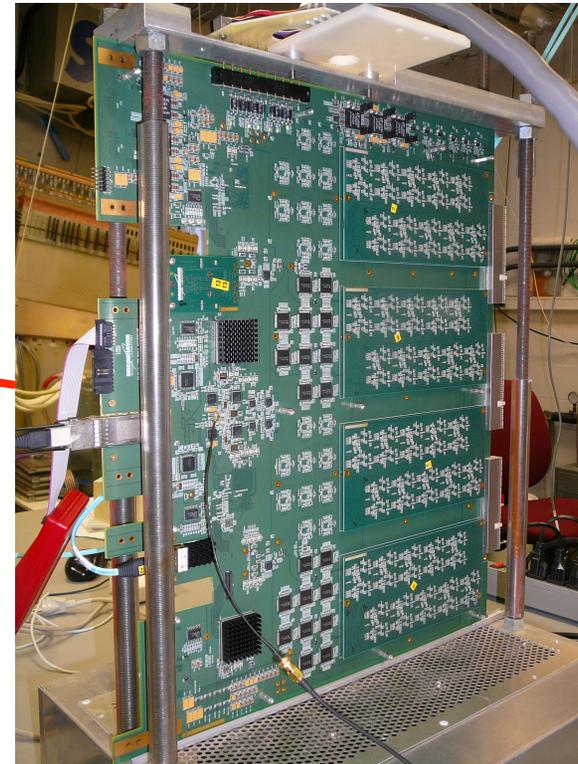
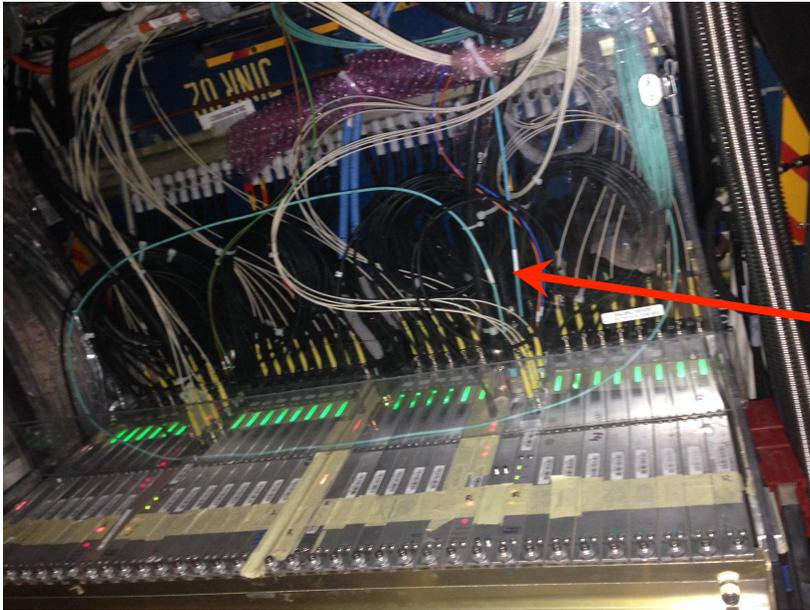
- BNL is actively involved in the ATLAS Phase-I upgrade
- BNL is a main contributor to each of the three subsystems in Phase-I Upgrade
  - *Liquid Argon Calorimeter*
  - *Muon New Small Wheel*
  - *TDAQ System*

# LAr Phase-I Upgrade



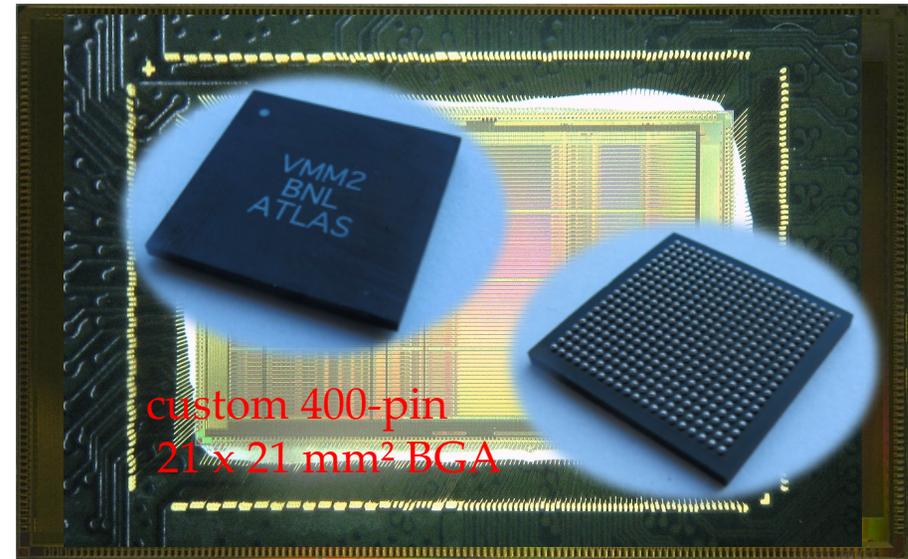
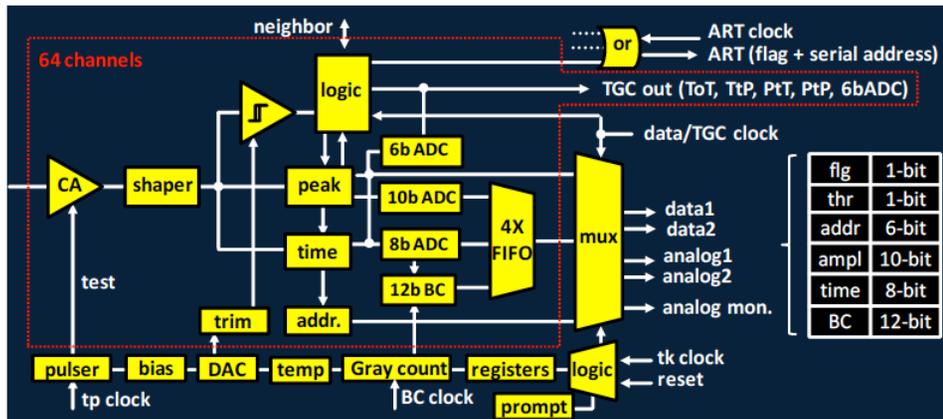
- **BNL is leading the architecture design of Phase-I LAr trigger electronics upgrade**

# Liquid Argon Trigger Digitizer Board



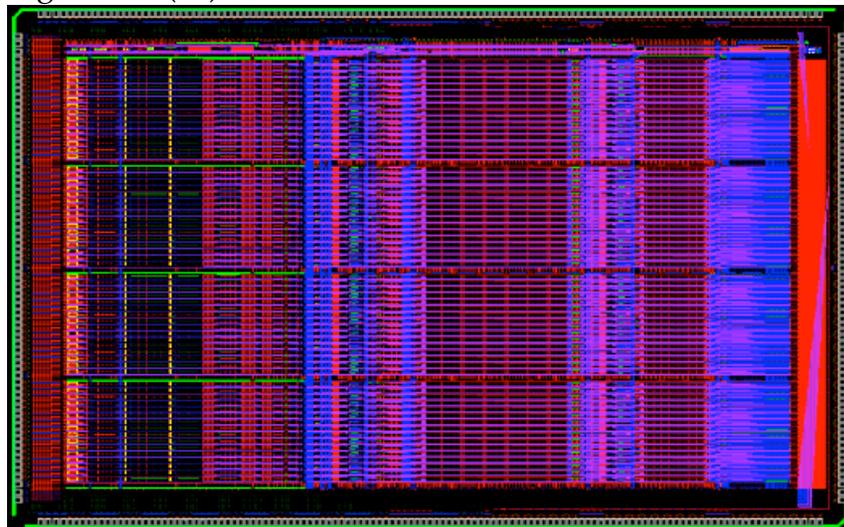
- LTDB is a front end board to digitize trigger signals on detector
  - High density – 320 super cell signals
  - High speed digitization – 40 Msps
  - High speed data transmission – 40 optical links running at 5 Gb/s
- LTDB demonstrator has been successfully installed on detector in July 2014
  - Data taken in I06 FEC ( $\Delta\eta = 0-1.4$ ,  $\Delta\phi = 1.8-2.2$ ) shows satisfactory performance

# Front End ASIC for Muon New Small Wheel



analog, mixed-signal, digital supplies (1.2V) – neigh.t – digital IOs (14) - TGC outs 0-6

64 inputs, 9 preamplifier supply (1.2V)



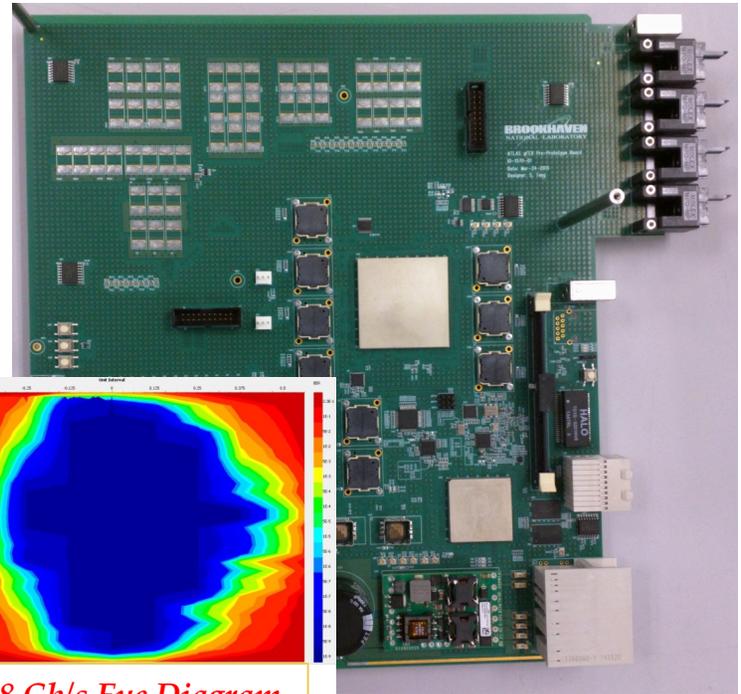
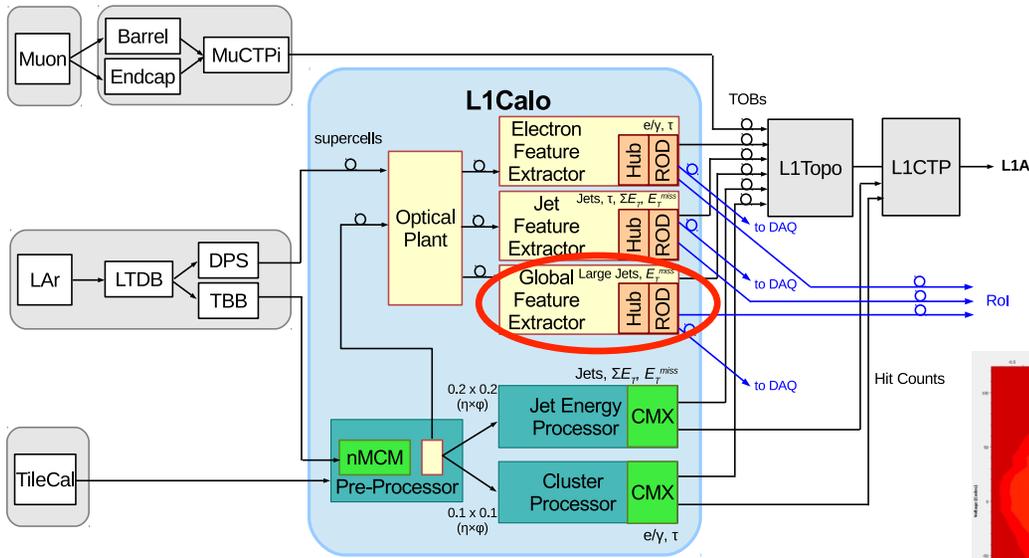
analog, mixed-signal, digital supplies (1.2V) – neigh.b – TGC outs 43-63 13.5 mm **392 bonding pads**

TGC outs 7-42

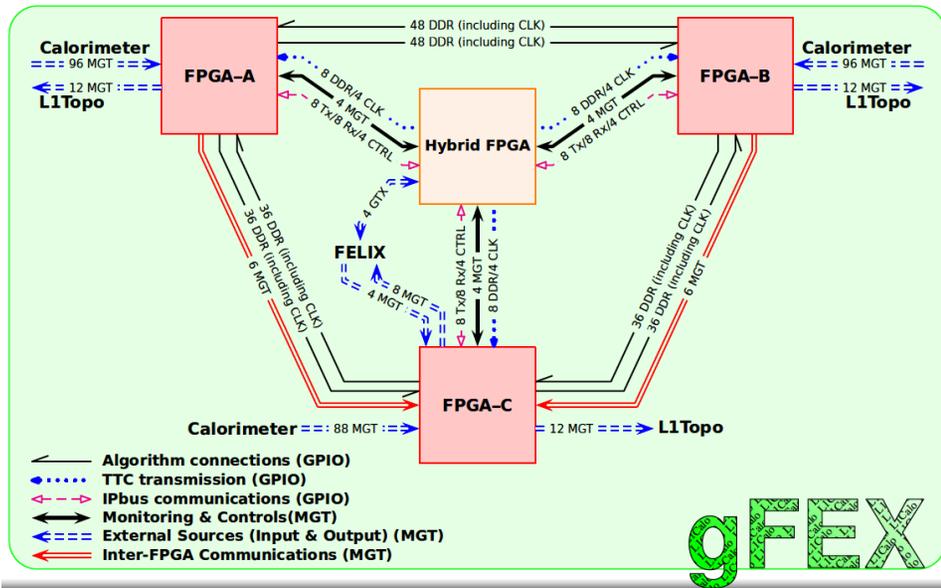
## VMM Chip

- Versatile front end ASIC for micro-pattern gas detectors
- Suitable for both MicroMegs and sTGC in Muon NSW
- Mixed-signal design, handle both signal polarities
- **64 channels** with integrated ADCs for peak amplitude measurement, sub-nanosecond time measurement and triggers
- Low power, **4-8 mW/channel** depending on features used
- CMOS 130 nm, 13.5 x 8.3 mm<sup>2</sup>, **over 5 million transistors**

# Global Feature Extractor in L1Calo

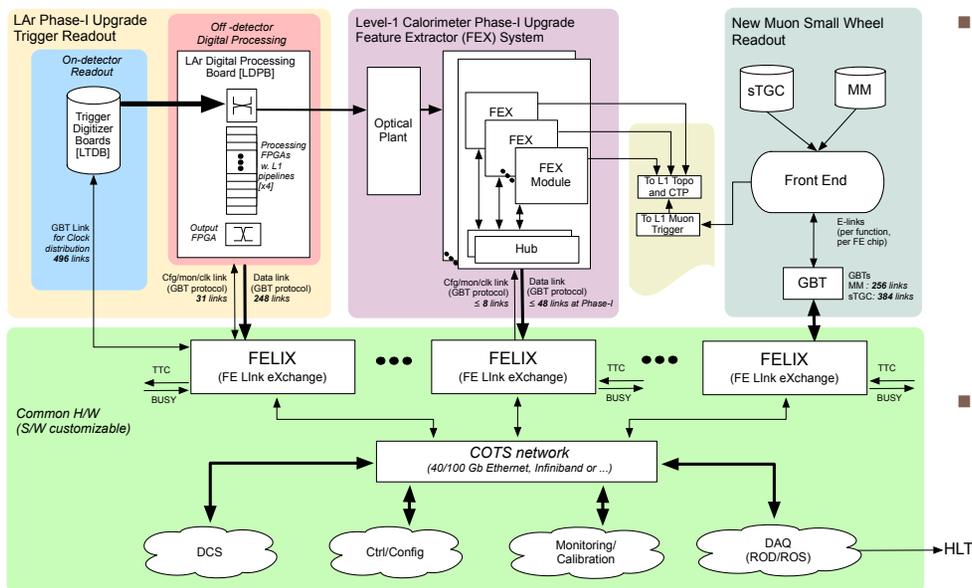


12.8 Gb/s Eye Diagram

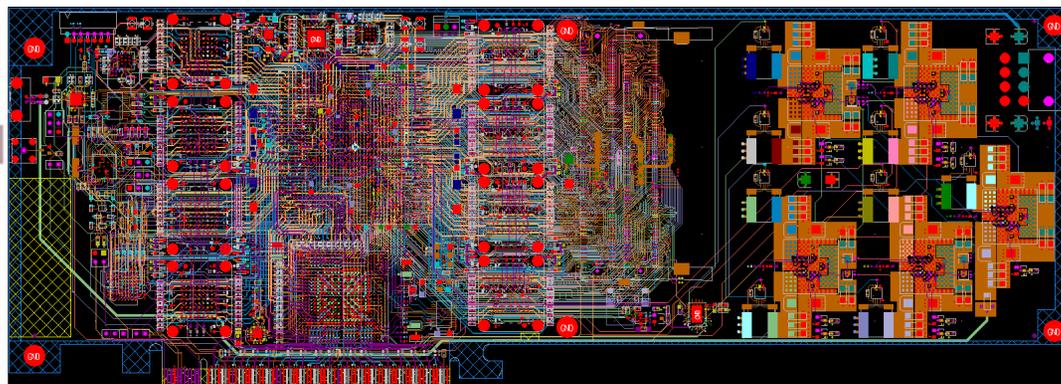
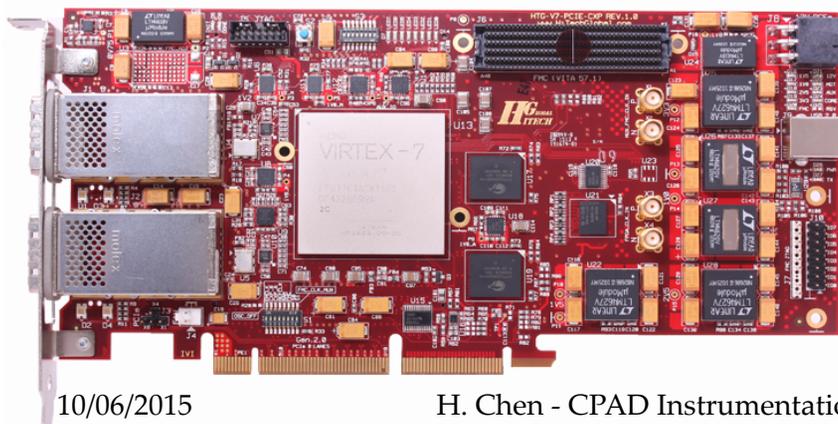


- gFEX is a single ATCA module to process entire ATLAS calorimeter information for large-R jet finding
  - High density optical I/O – 280 input links from Calorimeters
  - High speed optical link – 6.4 Gb/s to 12.8 Gb/s
  - Fast data processing in FPGA for jet finding – 5 BCs or 125 ns
- Excellent link performance on gFEX Prototype
  - IBERT at 12.8 Gb/s with  $< 1.2 \times 10^{-15}$  BER with **all 80 Virtex-7 GTH** and **all 16 Zynq GTX** running **simultaneously**

# Front End Link eXchange



- FELIX is a new approach to interface on-detector electronics in ATLAS TDAQ upgrade
  - It separates the Front End link interfacing from the Front End data processing.
  - It eliminates the static point-to-point connections between the Front Ends and the Read Out system.
  - This allows use of high bandwidth commercial network technology for data aggregation, transport and distribution
- BNL is developing GBT link firmware for FELIX, to interface to Front End system directly
  - Design is based on COTS PCIe Gen3 FPGA module
  - A PCIe card developed for LAr Phase-I upgrade is being explored for the FELIX use case

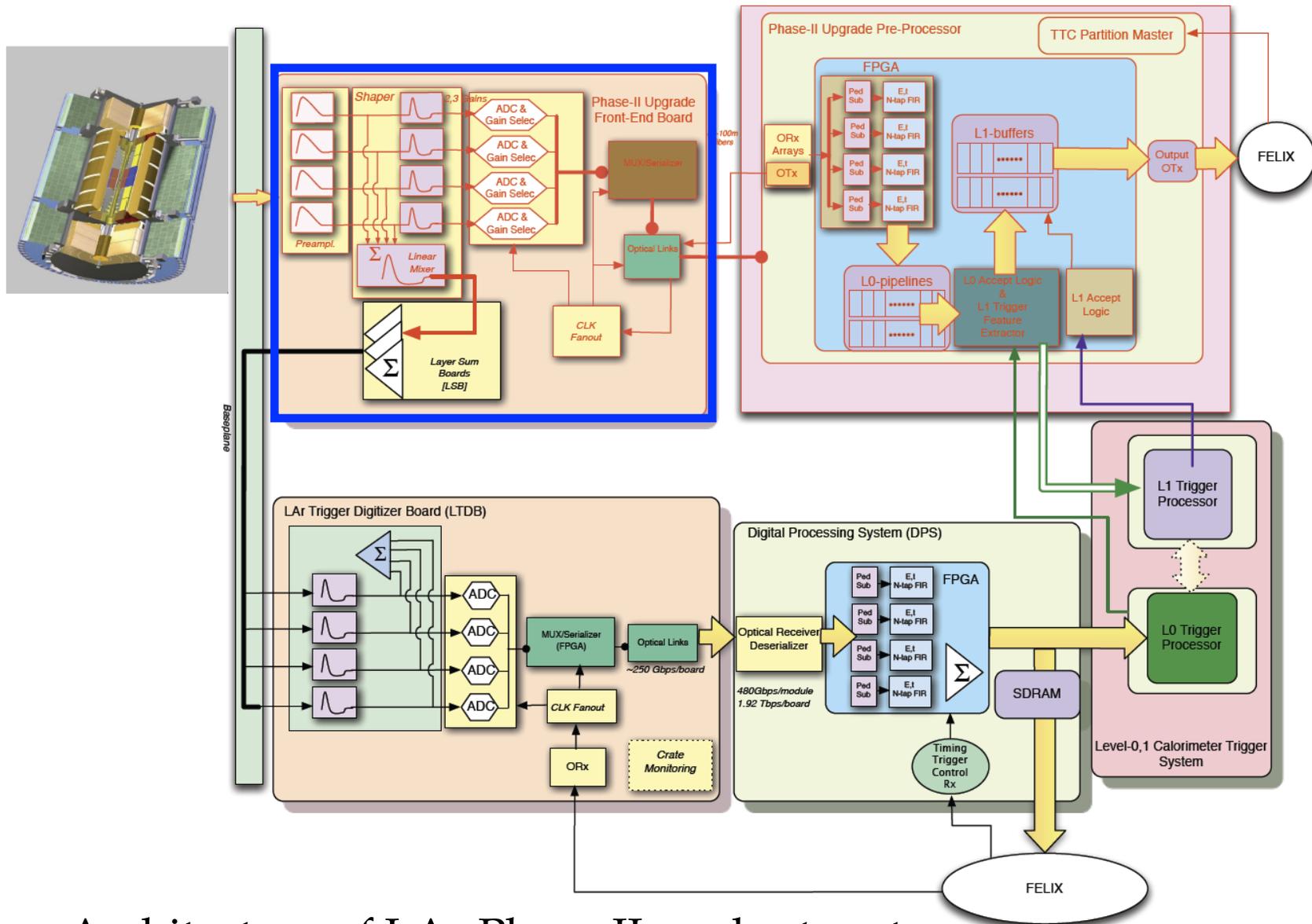


10/06/2015

H. Chen - CPAD Instrumentation Frontier Meeting

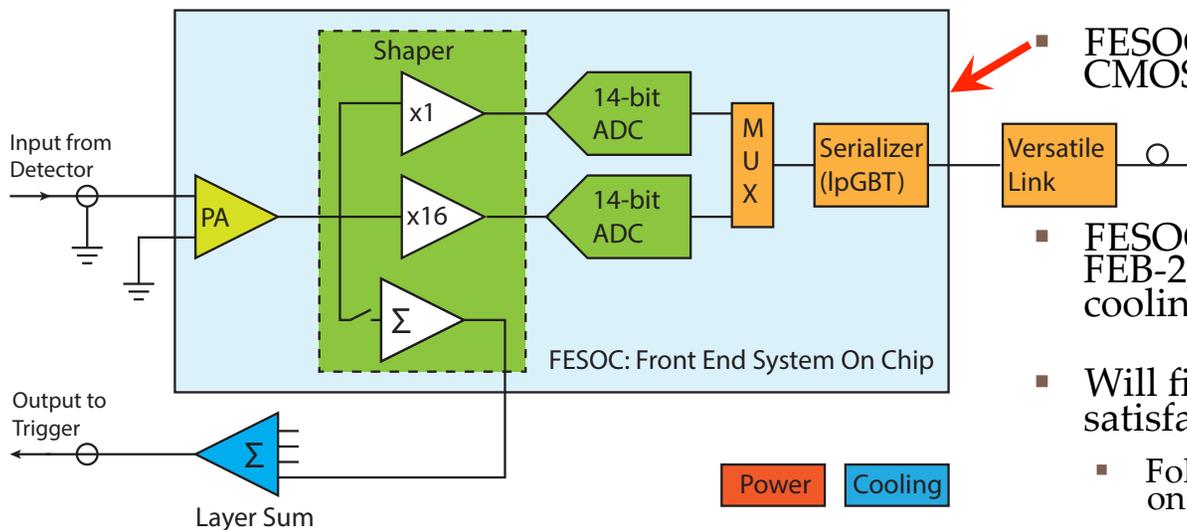
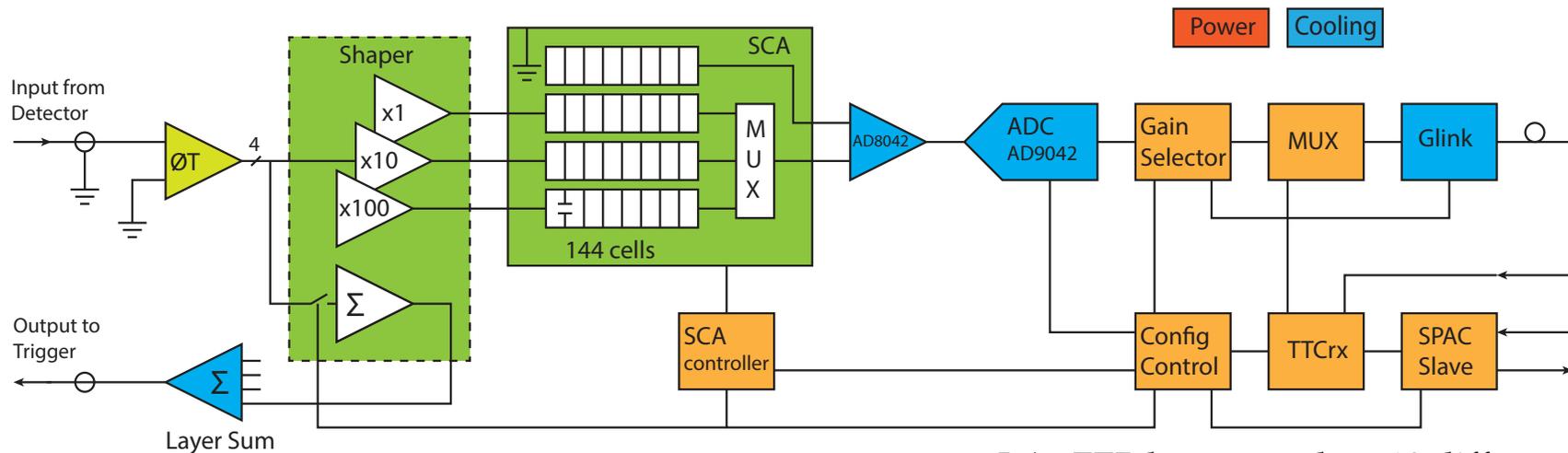
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# LAr Phase-II Upgrade



- Architecture of LAr Phase-II readout system

# From LAr FEB to FEB-2



- LAr FEB has more than 10 different ASICs designed in 4 different technologies
  - *Can we do better in Phase-II upgrade?*
- FESOC (Front End System on Chip) in 65nm CMOS technology
- FESOC will greatly simplify the design of FEB-2, and ease the system power and cooling management
- Will first demonstrate analog front end with satisfactory performance
  - Followed by the integration of 12-bit/14-bit ADC on chip
  - Final FESOC will use lpGBTx IP core currently being developed at CERN

# Summary – Hadron Collider Experiment

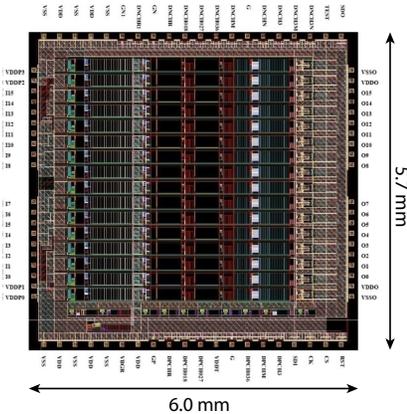
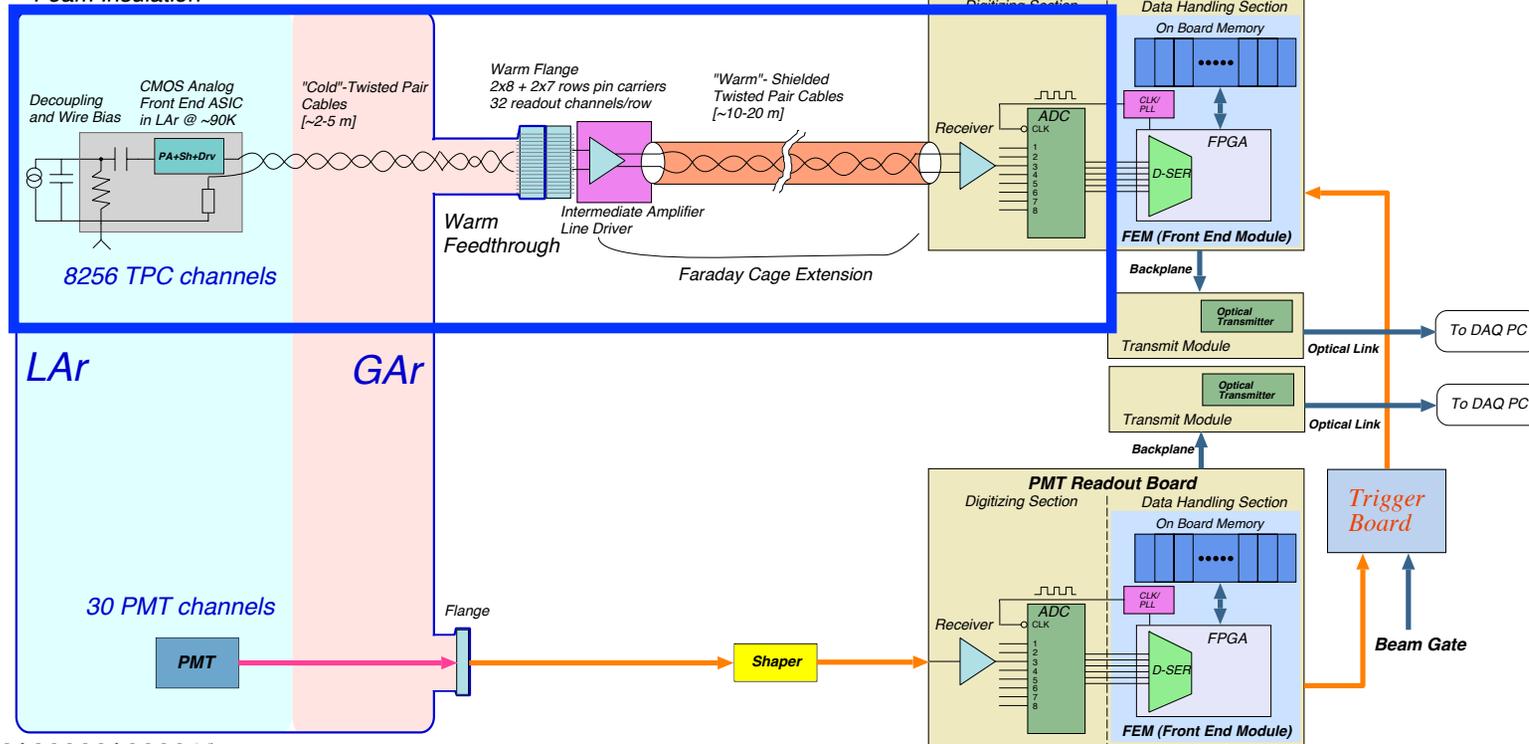
- **LAr Calorimeter Trigger Electronics in Phase-I ATLAS Upgrade**
  - ~40,000 super cell signals, digitized on detector with high speed, low power, rad-hard ADC
  - ~25TeraBit/s of data is streamed out of detector continuously through parallel fiber optical links
  - High speed, real time, parallel digital signal processing in modern FPGA for calorimeter trigger generation
- **New Small  $\mu$ -Wheel in Phase-I ATLAS Upgrade**
  - Front end chip with versatile functionalities to meet different detector technologies (both Micromegas and sTGC)
  - On chip charge and time digitization, buffering and multiplexing into a high speed serial link
  - Industry standard link interface to connect directly to a computer eliminating any additional conventional DAQ hardware
- **Trigger/DAQ System in Phase-I ATLAS Upgrade**
  - A single module with high density optical transmission and parallel DSP in FPGA to process whole ATLAS calorimeter information to produce large-R jet trigger
  - Innovative DAQ platform based on high speed parallel fiber optical link and PCIe Gen3 hardware to eliminate conventional DAQ hardware
- **ATLAS LAr Phase-II Upgrade**
  - Development of front end electronics will focus on 65nm based FESOC
  - Will greatly simplify the system design and overall power management

Noble Liquid TPCs for Neutrino  
Experiments:  
Low Noise Multiplexed Readout  
integrated on the TPC electrodes

# MicroBooNE Front End Electronics (1)

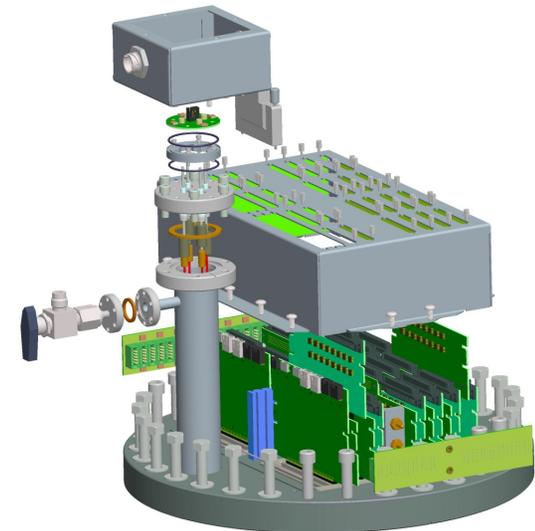
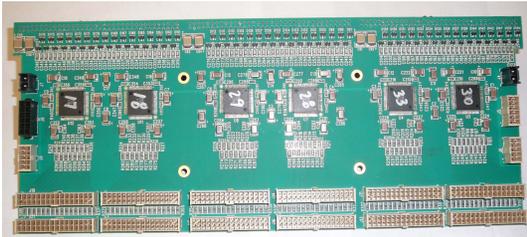
DAQ in Detector Hall

Single Vessel Cryostat with 8-10% Ullage  
Foam Insulation

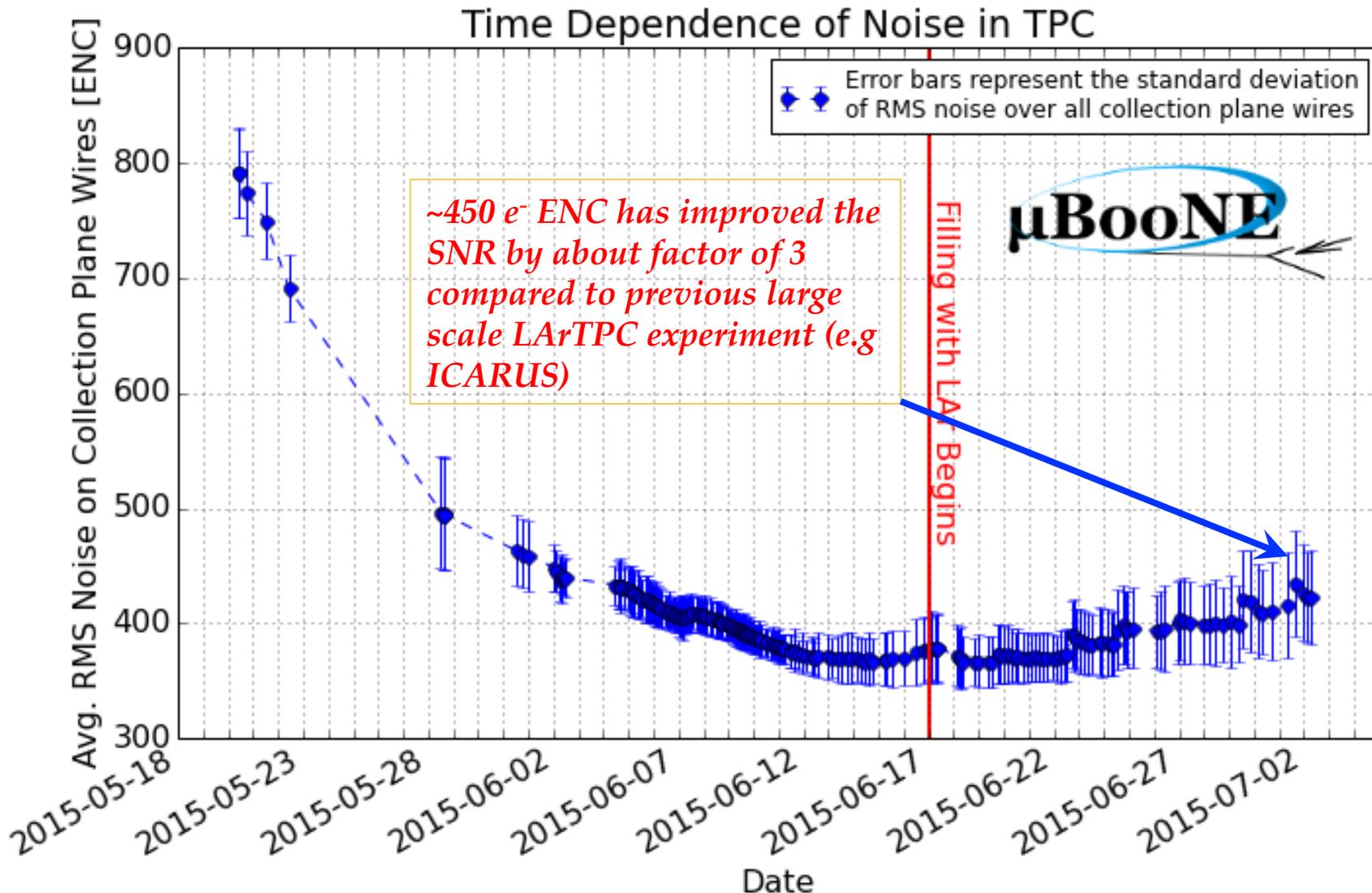


- BNL designed front end readout electronics system for MicroBooNE experiment
- Analog front end ASIC designed in 180 nm is running in LAr (~89 K) to achieve optimum signal to noise ratio
- MicroBooNE is the first experiment instrumented with cold CMOS ASICs

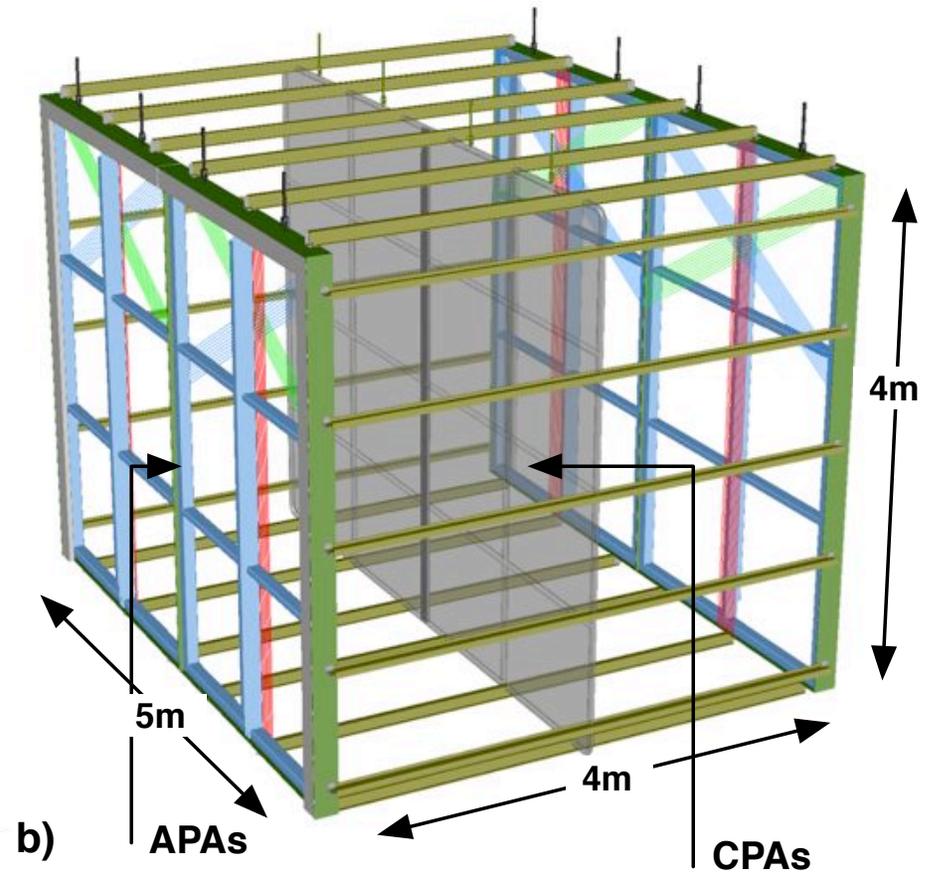
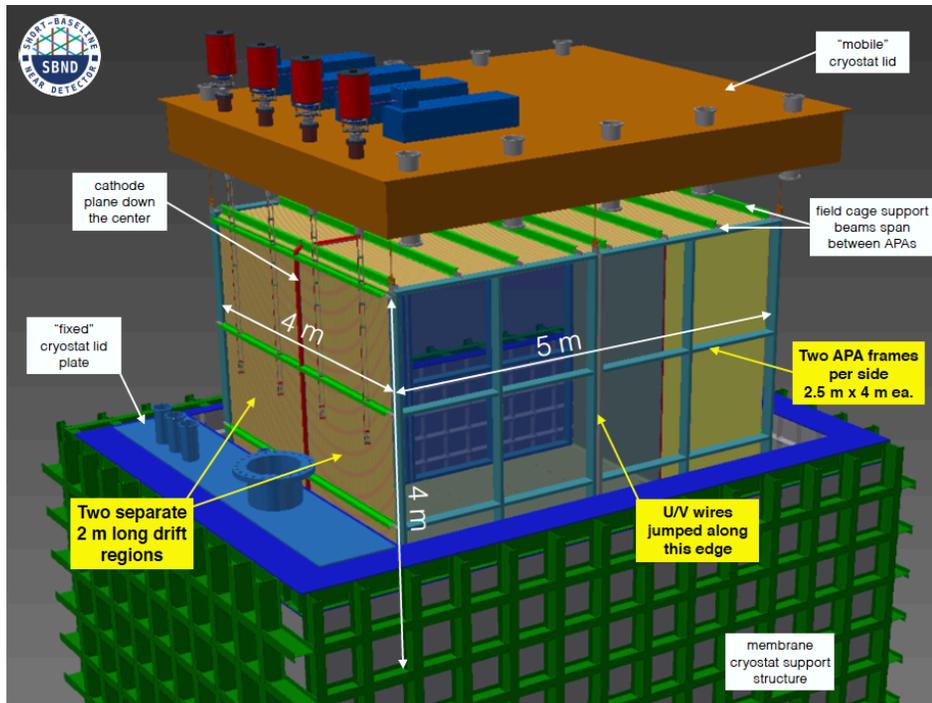
# MicroBooNE Front End Electronics (2)



# MicroBooNE Cold Electronics Temperature Dependence of Noise in TPC

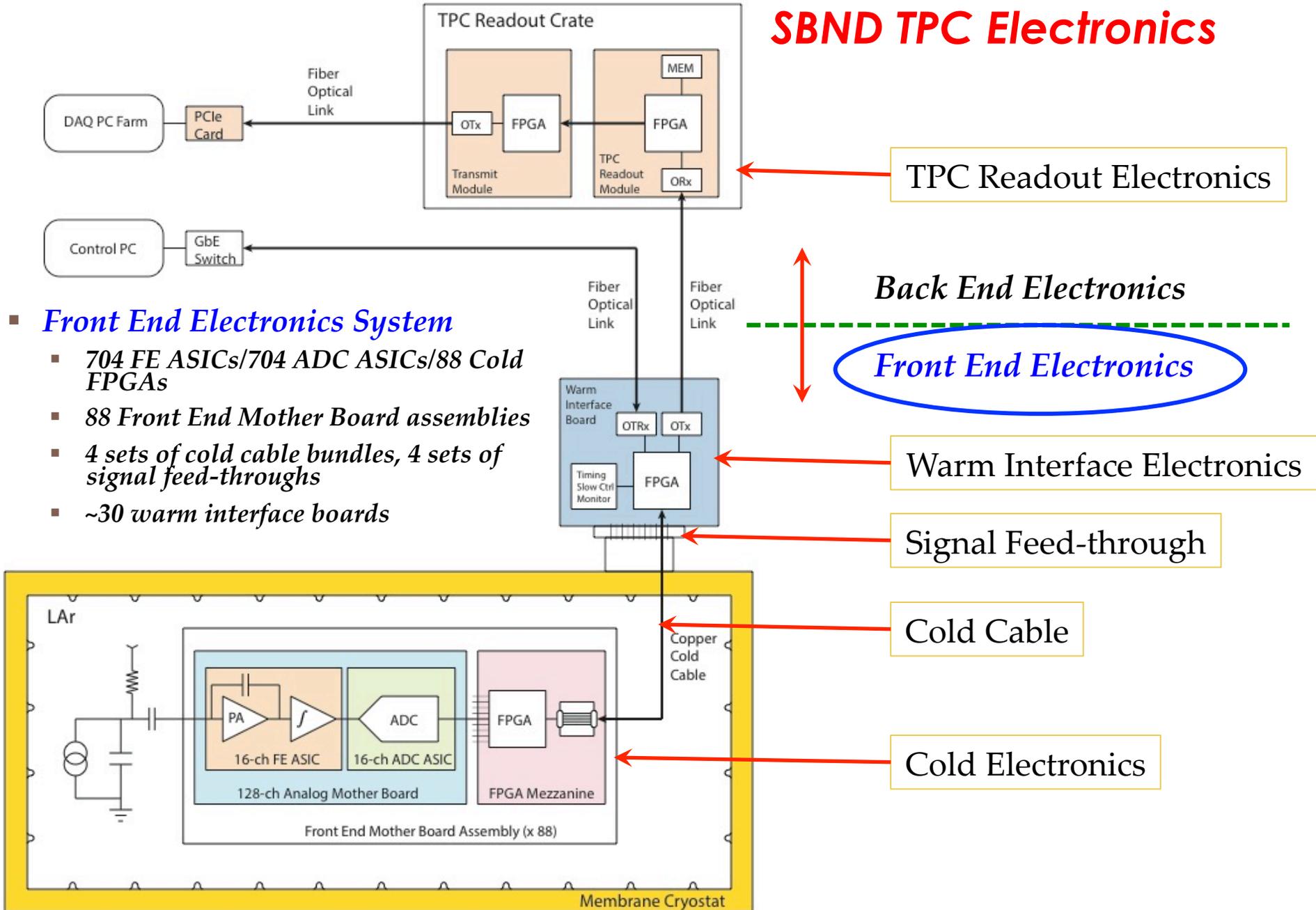


# SBND Experiment



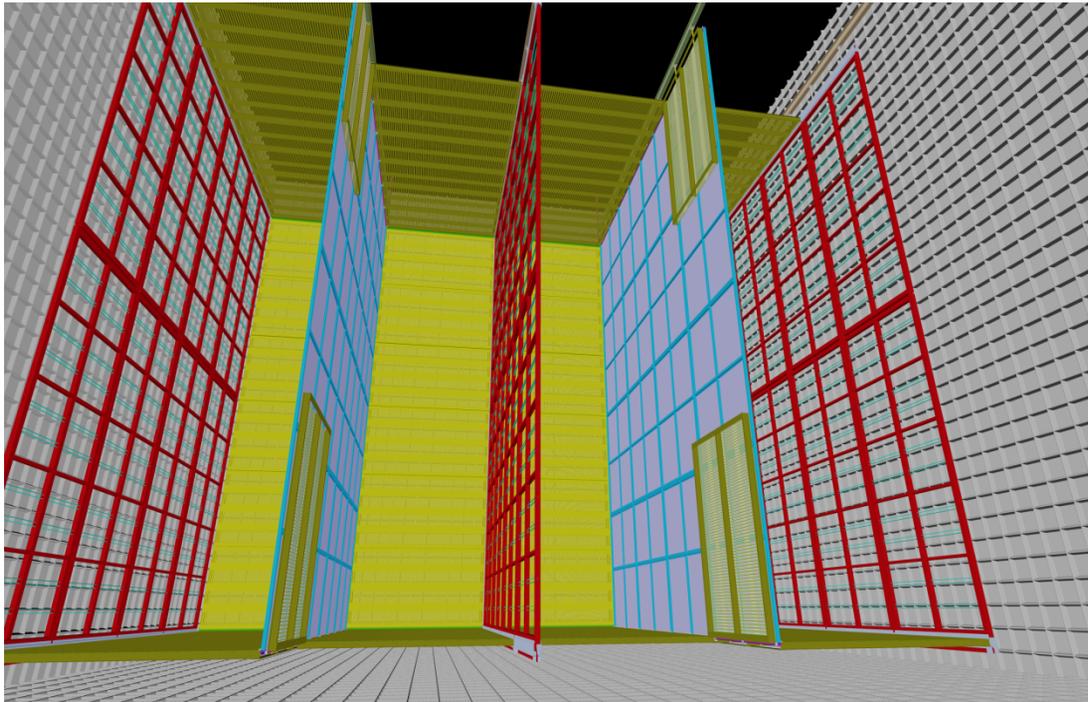
- SBND TPC: 4 Anode Plane Assemblies and 2 Cathode Plane Assemblies
  - Total 11,264 channels (sense wires)
- BNL is developing APA & front end readout electronics system for SBND TPC

# SBND TPC Electronics

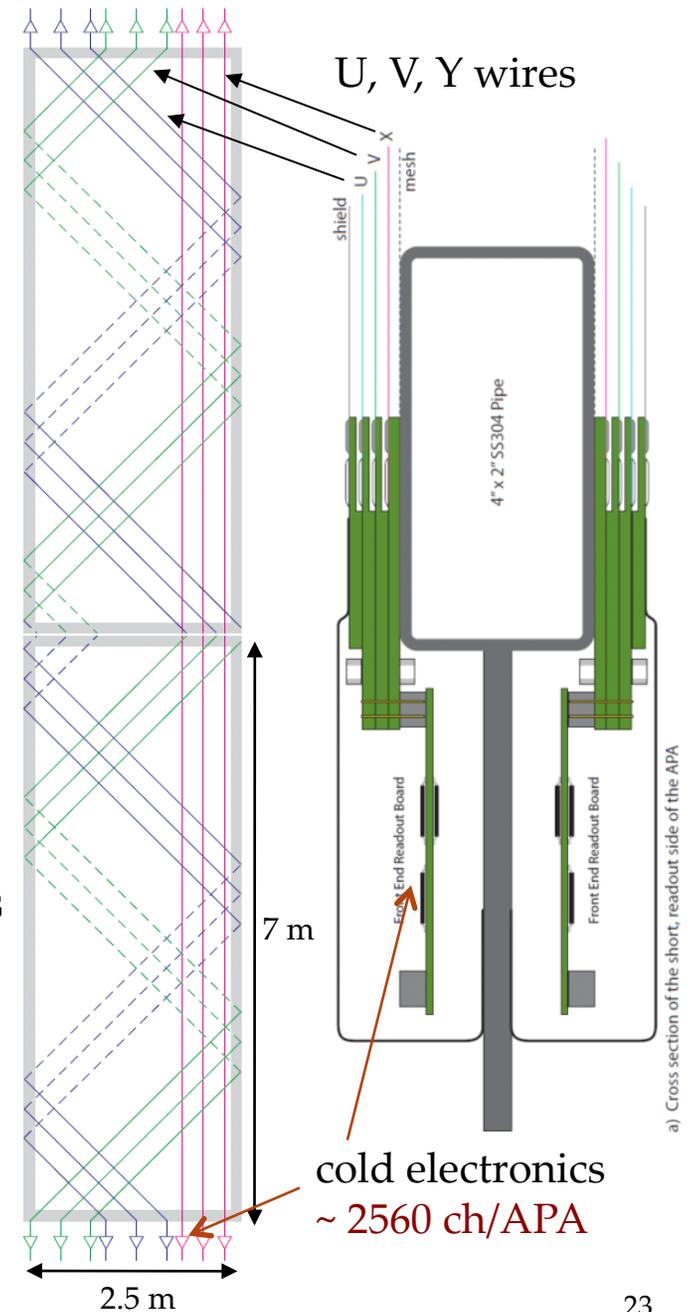


- **Front End Electronics System**
  - 704 FE ASICs/704 ADC ASICs/88 Cold FPGAs
  - 88 Front End Mother Board assemblies
  - 4 sets of cold cable bundles, 4 sets of signal feed-throughs
  - ~30 warm interface boards

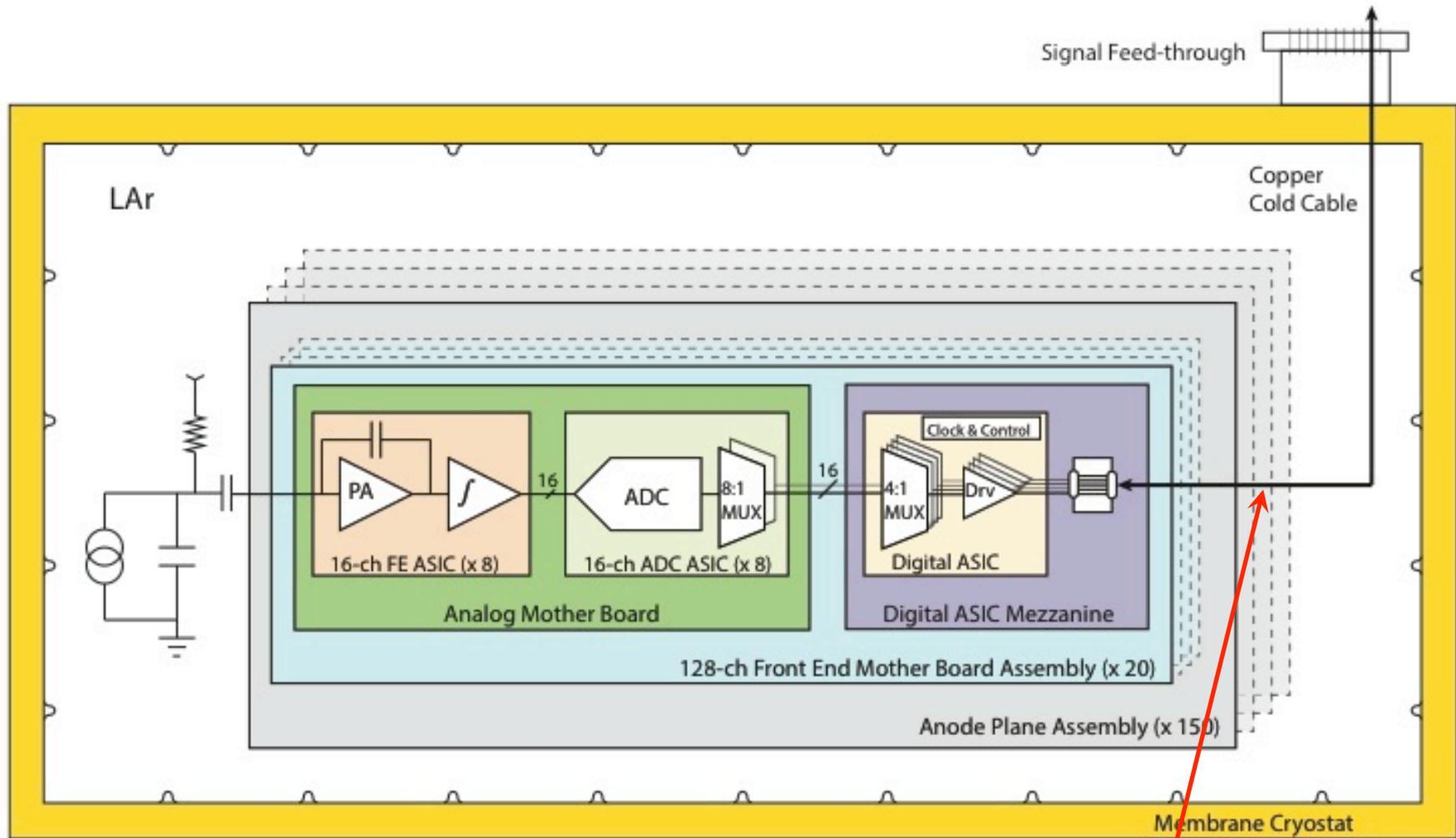
# Cold Electronics for DUNE Far Detector



- BNL is developing APA & front end cold electronics system for DUNE far detector
- DUNE 10 kt Far Detector
  - **384,000 channels**
  - 24,000 FE ASICs/24,000 ADC ASICs
  - 6,000 COLDATA ASICs (FNAL)
  - 3,000 Front End Mother Board assemblies



# DUNE FD TPC Readout Electronics

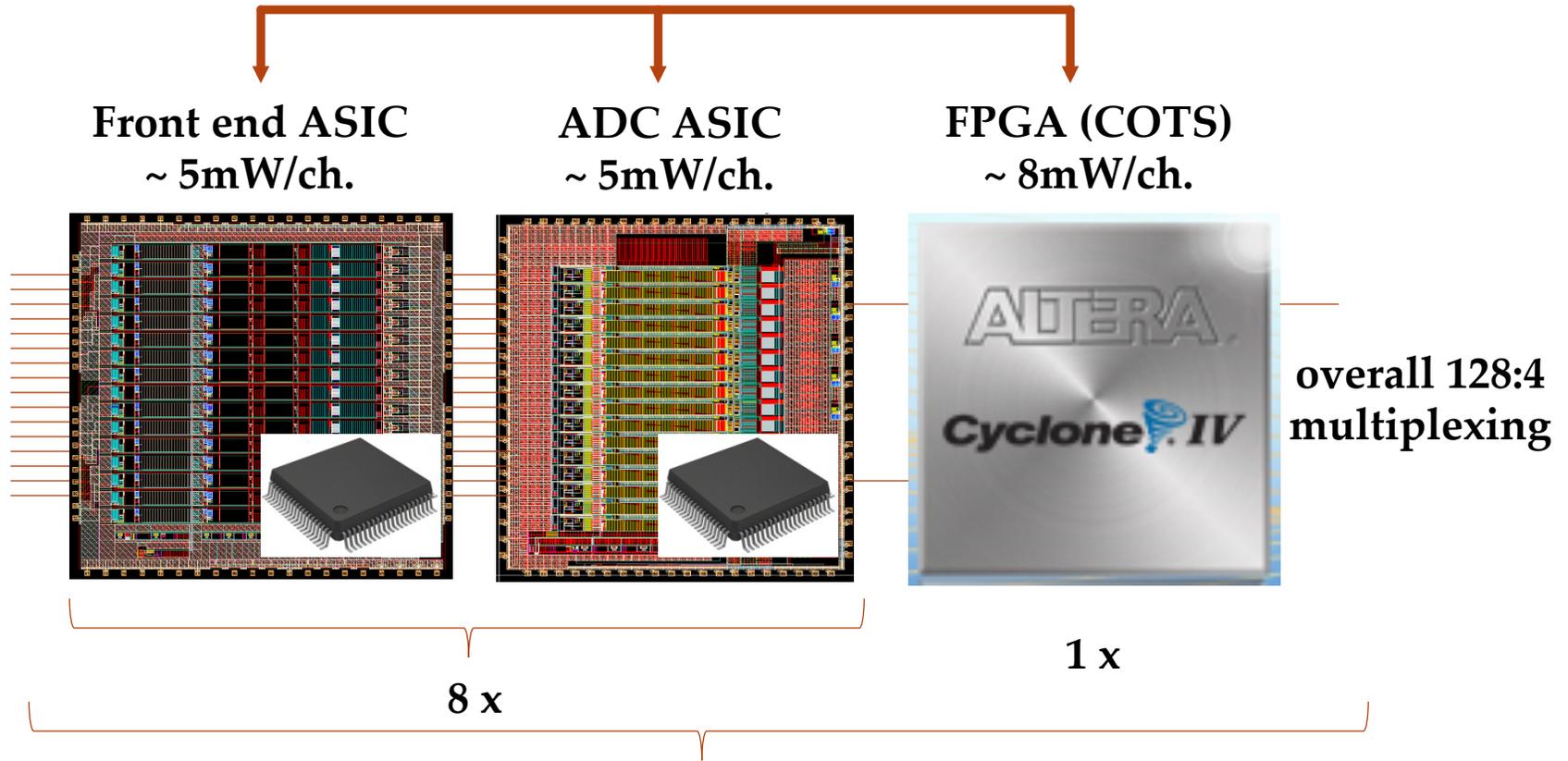


1 Gb/s data link x 4

# Cold Electronics



voltage regulation  
(COTS)  
( $< 100\text{mV}$  dropout)



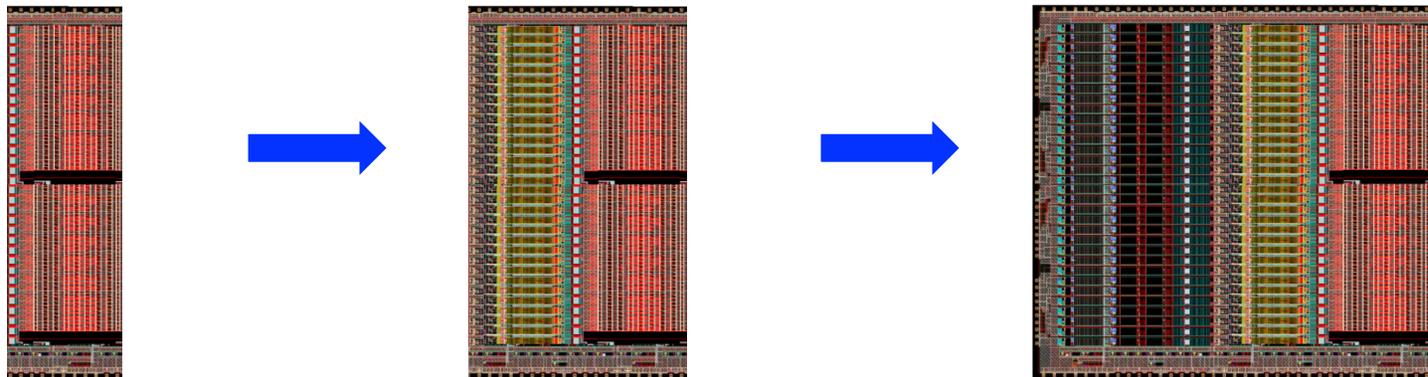
*A Complete Front End  
Readout Chain  
for SBND and DUNE  
Far Detector TPC*



Front end mother  
board assembly  
serving 128 wires  
 $\sim 2.4\text{ W}$

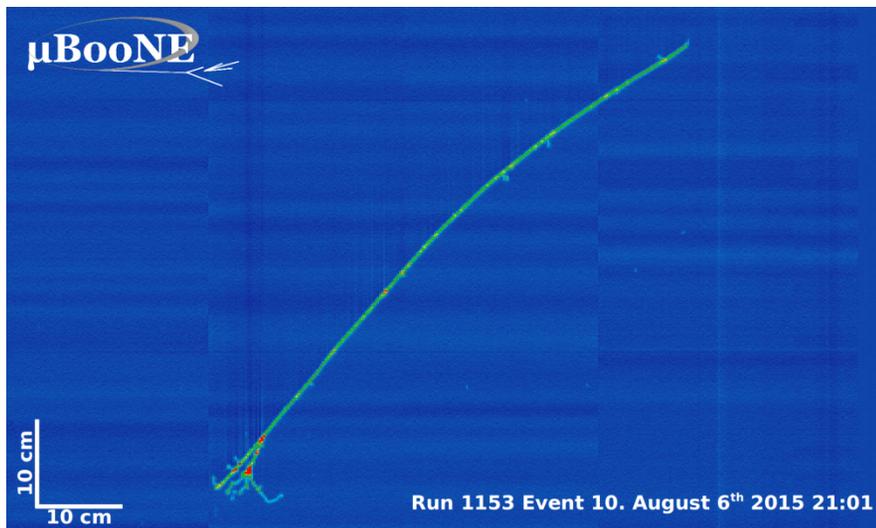
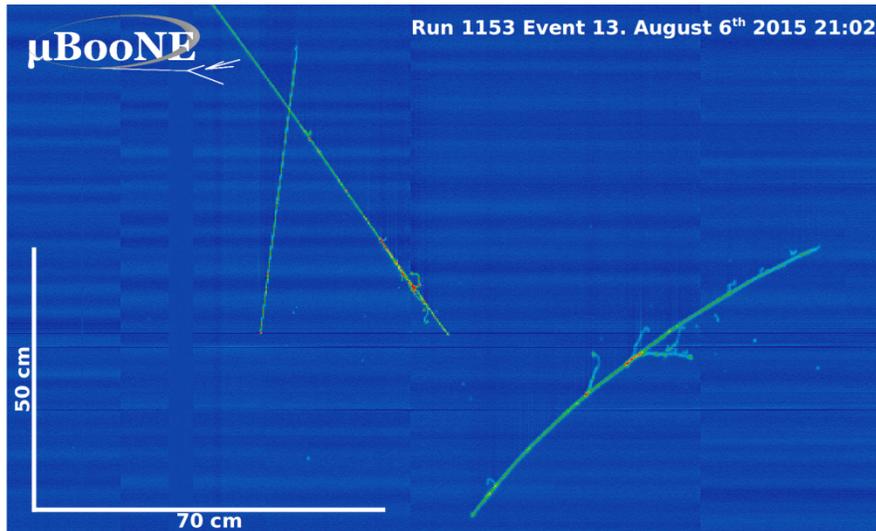
# Fully Integrated Cold ASIC

- An alternative plan is being considered, to explore a development path to better optimized system
- A 32-channel fully integrated ASIC can be developed for LArTPC, it will have
  - 32-ch preamplifier and anti-alias shaper
  - 32-ch 2 MS/s 12-bit low power ADC
  - 1-ch serializer for data transmission @ 1 Gb/s
- This will be leveraging past development efforts and expertise from cold FE and ADC ASIC development since 2008
  - ADC ASIC that was developed is not just a simple multi-channel ADC, but it also provides S/H at the input and buffering, multiplexing and serialization at the output
  - The multiplexing degree and channel number can also be increased, if the application requires
- A full integrated ASIC opens the door to other possibilities, can be used in other experiments (e.g.  $0\nu\beta\beta$  experiment nEXO for charge readout)



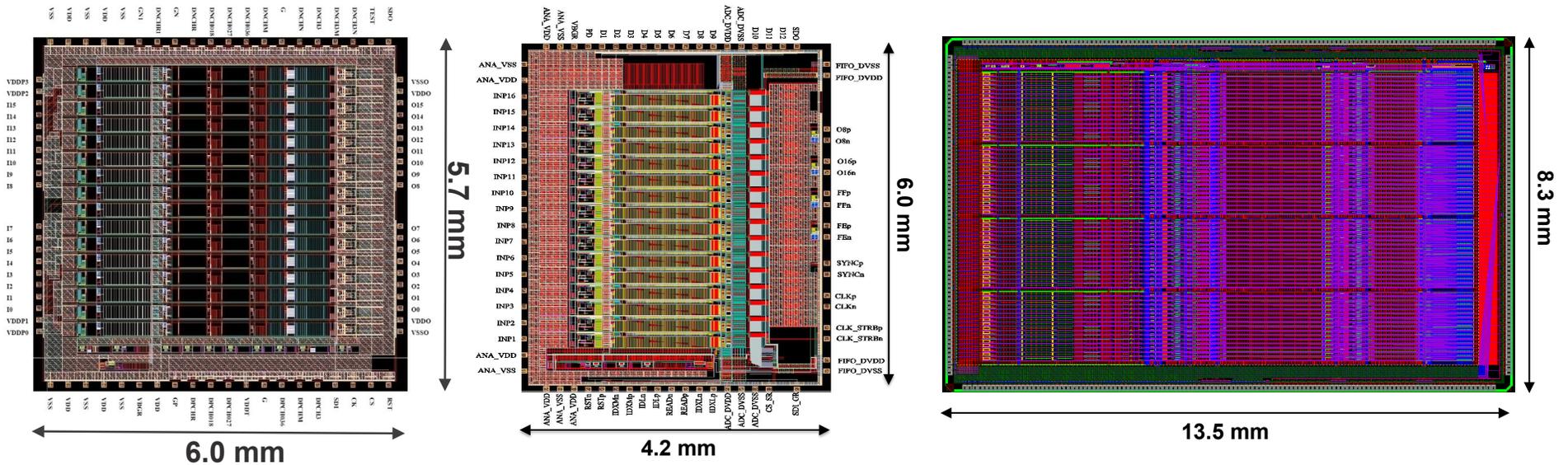
*Develop PLL and serial link → 32-ch ADC with PLL and serial link → Fully integrated 32-ch cold ASIC*

# Summary – Readout of Noble Liquid TPCs



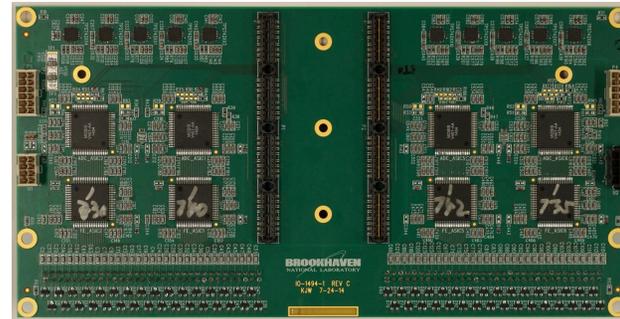
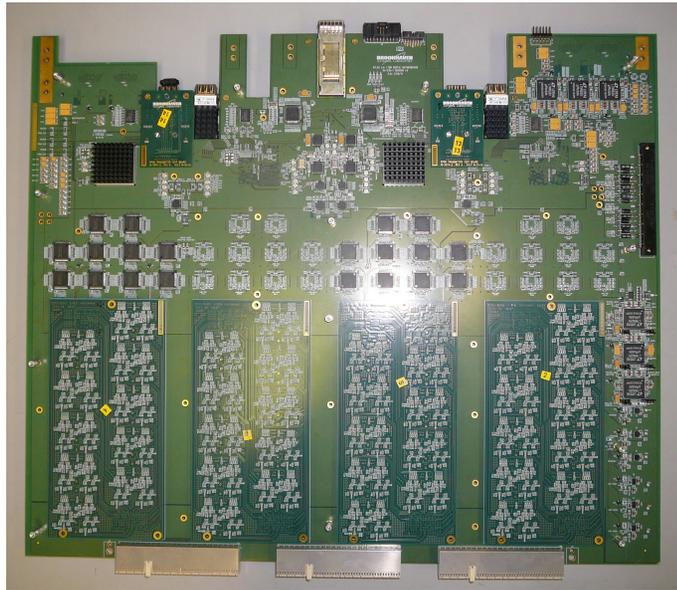
- Readout electronics developed at BNL for low temperatures (77K-300K) is an *enabling* technology for noble liquid and mixed phase detectors for neutrino and dark matter research
- Cold electronics decouples the electrode and cryostat design from the readout design. With electronics integral with detector electrodes the noise is independent of the fiducial volume (signal cable lengths), and much lower than with warm electronics.
- Signal *multiplexing* results in large reduction in the quantity of cables (less outgassing) and the number of feedthroughs/cryostat penetrations.
- MicroBooNE is the first running experiment instrumented with CMOS cold electronics
- Full cold readout chain with FE ASIC, ADC ASIC and FPGA/COLDATA will be used to equip the SBND and DUNE LAr TPC

# Concluding Remark (1)



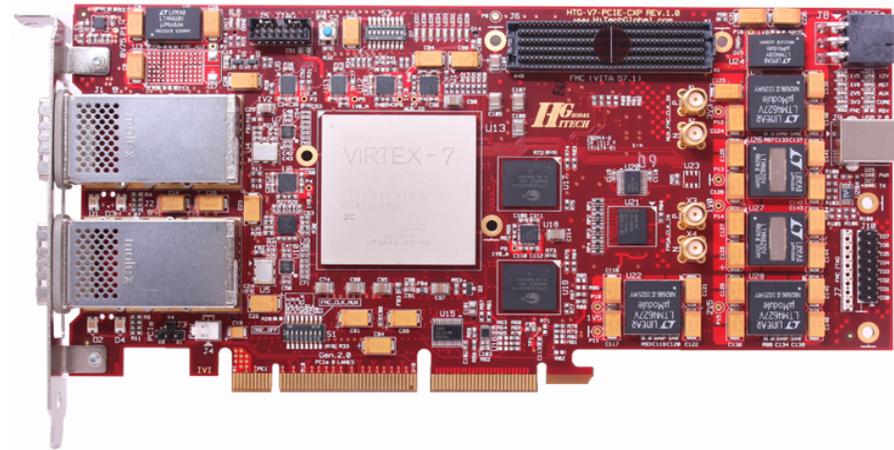
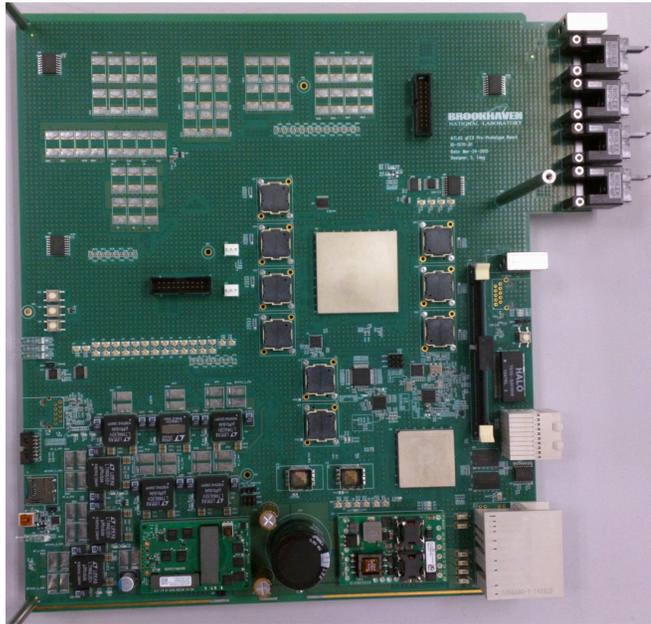
- Front end ASIC design is optimized for detector technologies
- 
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# Concluding Remark(2)



- Front end ASIC design is optimized for detector technologies
- Front end board design is tailored for experimental environment (radiation, cryogenic temperature etc.)
-

# Concluding Remark (3)



- Front end ASIC design is optimized for detector technologies
- Frontend board design is tailored for experimental environment (radiation, cryogenic temperature etc.)
- Trigger/DAQ design explores the ultimate use of COTS solution (high speed optical link, DSP in FPGA etc.)

# Concluding Remark (4)

- *Expertise has been developed in R&D to provide an integrated solution of readout and Trigger/DAQ system for future experiments*
  - It is well aligned with P5 recommendation
  - A recent example is the proposal of readout system for SBND in Short Baseline Neutrino program → *short-term high priority project*
  - R&D in FESOC of ATLAS Phase-II Upgrade and Full Integrated Cold ASIC for TPC readout → *long-term R&D with high risk and high impact*



- Front end ASIC design is optimized for detector technologies
- Front end board design is tailored for experimental environment (radiation, cryogenic temperature etc.)
- Trigger/DAQ design explores the ultimate use of COTS solution (high speed optical link, DSP in FPGA etc.)

# Backup Slides

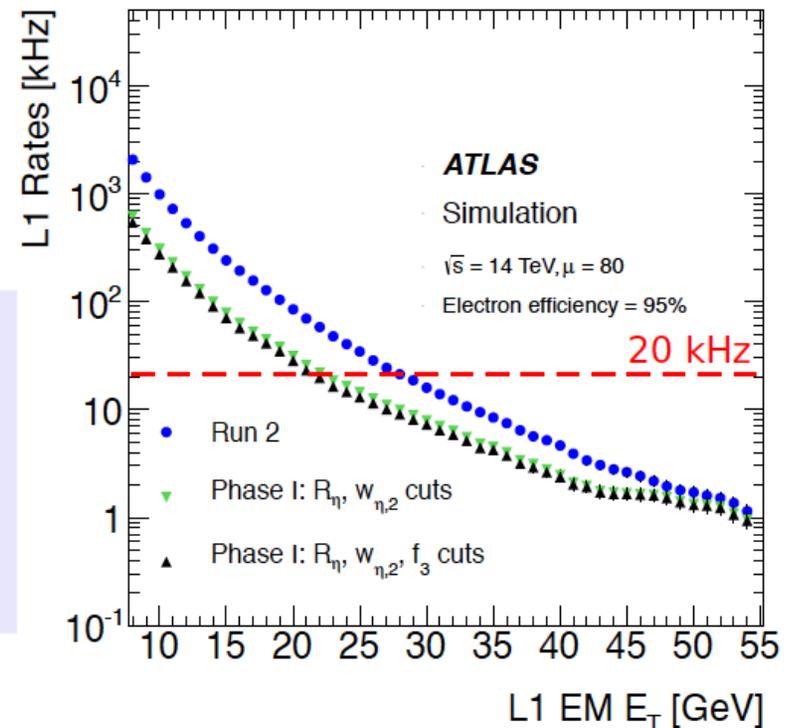
# Integrated Readout and Trigger/DAQ System

- With deep submicron technology (130 nm, or less) the ADC and powerful DSP processing can be integrated with the low noise front end to a greater extent than ever before
- Front-end optimized for each of different detector technologies
  - Low noise, low power analog front end: preamplifier, shaper etc.
- Analog-to-Digital Converters
  - Low power, high resolution and high density
- FPGA
  - FPGA (also for operation in LAr) with flexible algorithms for data processing and reduction
- Data Link
  - High speed serial link to unify the interface to back end system
  - It simplifies the interface to DAQ PC farm, minimizes or eliminates the conventional DAQ hardware

# ATLAS Phase-I Physics Motivation

- **Enhance trigger rejection while retaining efficiency**

- higher luminosity (up to  $3 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ )  $\Rightarrow$  higher trigger rates
- raising thresholds to contain rates results in significant loss of efficiency for events triggered on single leptons
- impacts  $W$ ,  $WH$ ,  $t\bar{t}$ , top, SUSY, ...
- Phase-I upgrades allow ATLAS to recover lost efficiency without exceeding rate limits



Level-1 trigger	Relative Eff. $WH \rightarrow l\nu b\bar{b}$	Trigger Rate (kHz)
<i>Muon channel</i>		
$p_T > 20 \text{ GeV}$ with current system	82	40
$p_T > 20 \text{ GeV}$ with Phase-I upgrade	78	18
<i>Electron channel</i>		
$p_T > 35 \text{ GeV}$ with current system	71	16
$p_T > 35 \text{ GeV}$ with Phase-I upgrade	71	6.5

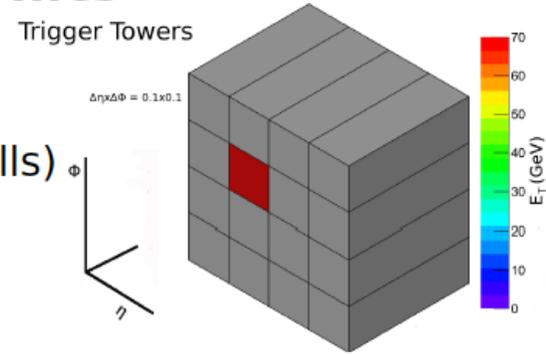
- **Phase-I Upgrades:**

- Fast-Tracker Trigger
- Muon New Small Wheel
- Liquid Argon Trigger Readout
- Trigger/DAQ Electronics

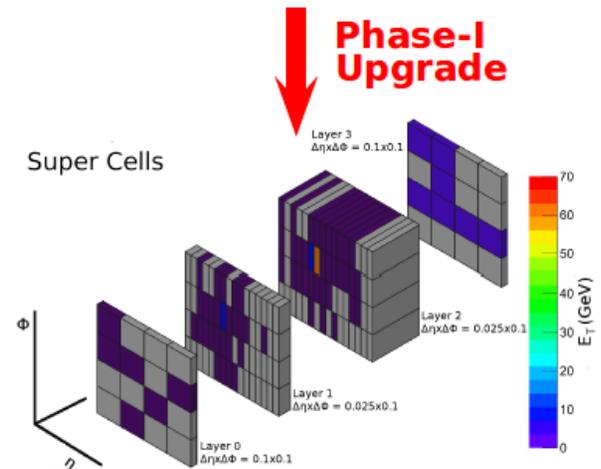
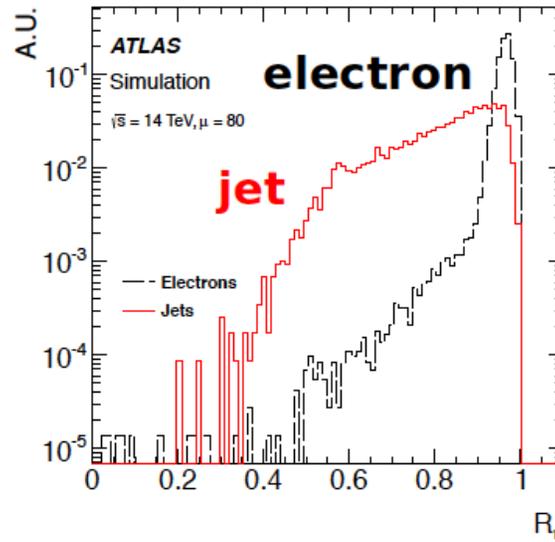
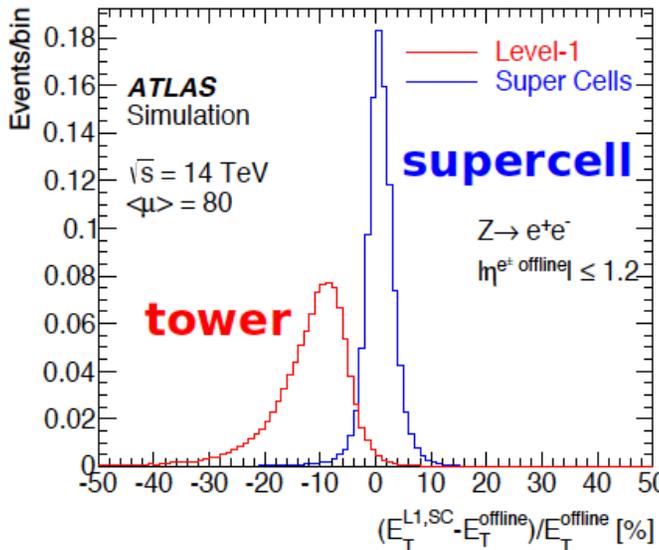
**BNL is a major contributor to the Phase-I Upgrade in our areas of core expertise**

# LAr Trigger Segmentation

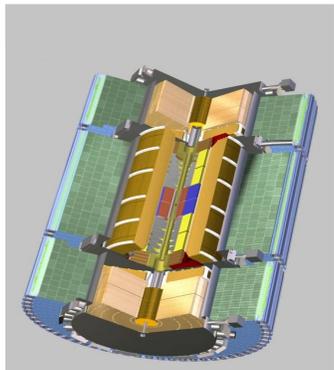
- **BNL proposed concept and overall design for Phase-I Upgrade of Liquid Argon calorimeter trigger electronics**
- **Increased granularity and functionality of LAr calorimeter Level 1 trigger**
  - fine lateral and longitudinal LAr segmentation (supercells)
  - calculate shape information for electrons and taus and improve energy measurement in the trigger readout chain to improve trigger rejection
  - detailed studies on supercell configuration and electron shower shapes by BNL



$$R_{\eta} = \frac{E_{T, \Delta\eta \times \Delta\phi = 0.075 \times 0.2}^{\text{layer 2}}}{E_{T, \Delta\eta \times \Delta\phi = 0.175 \times 0.2}^{\text{layer 2}}}$$



# Readout Architecture in Phase-I Upgrade

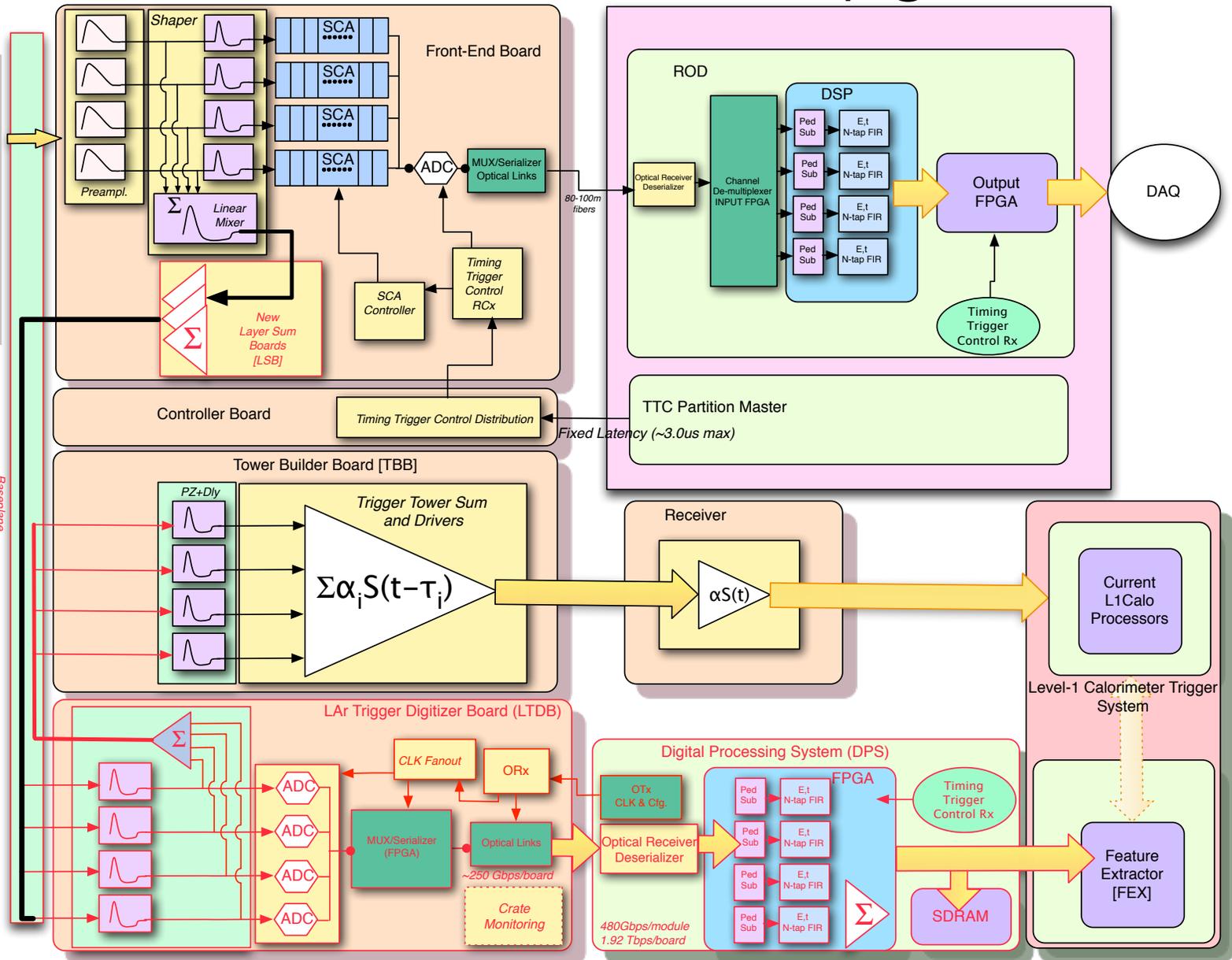


**Phase 0: ~0.5k super cells, 1.4x0.4 are on one FEC of the barrel calorimeter**

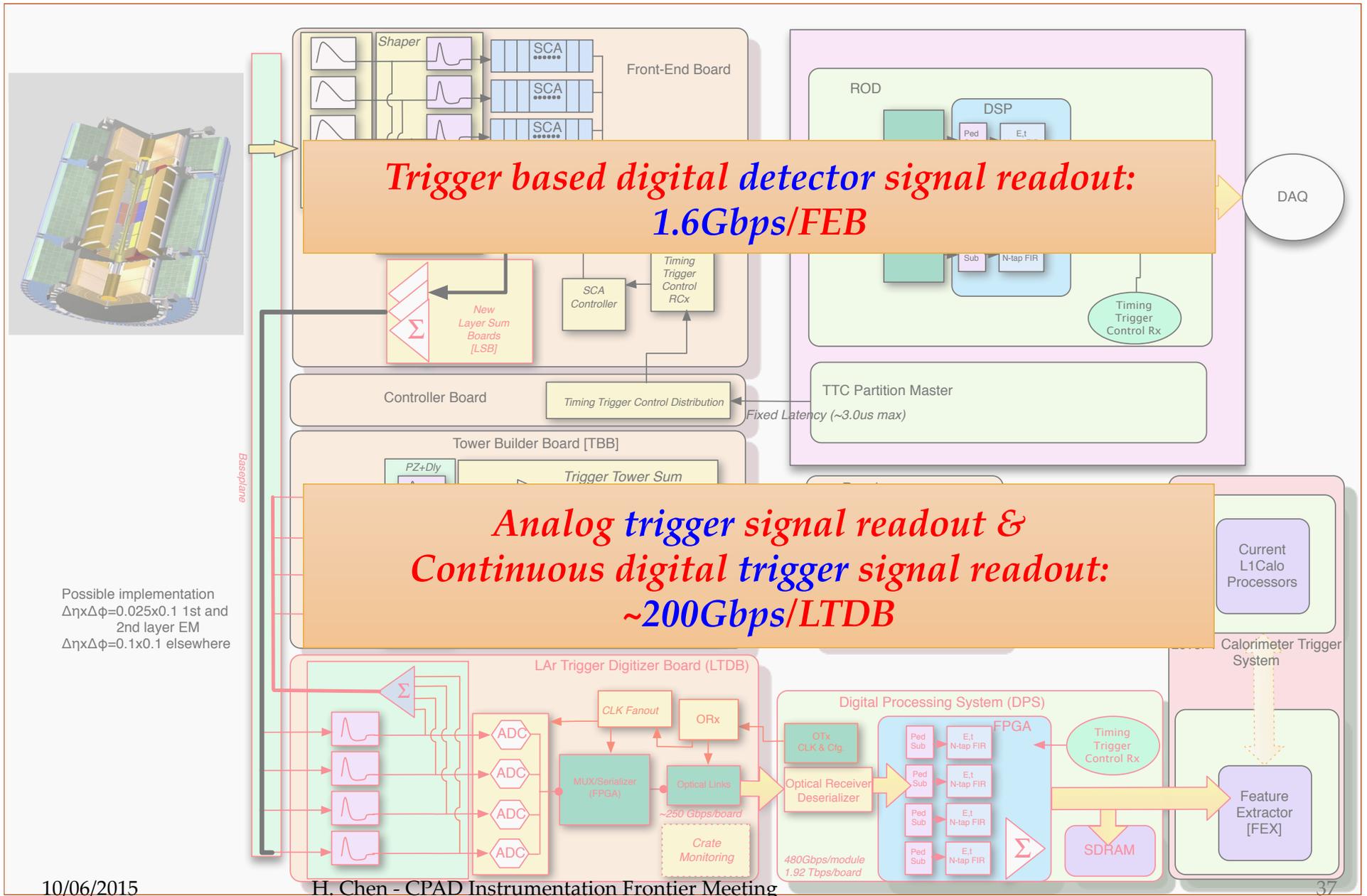
Possible implementation  
 $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$  1st and 2nd layer EM  
 $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$  elsewhere

**Phase-1: extend to the full calorimeter trigger readout (~35k channels), L1 trigger using digitized super cells**

10/06/2015

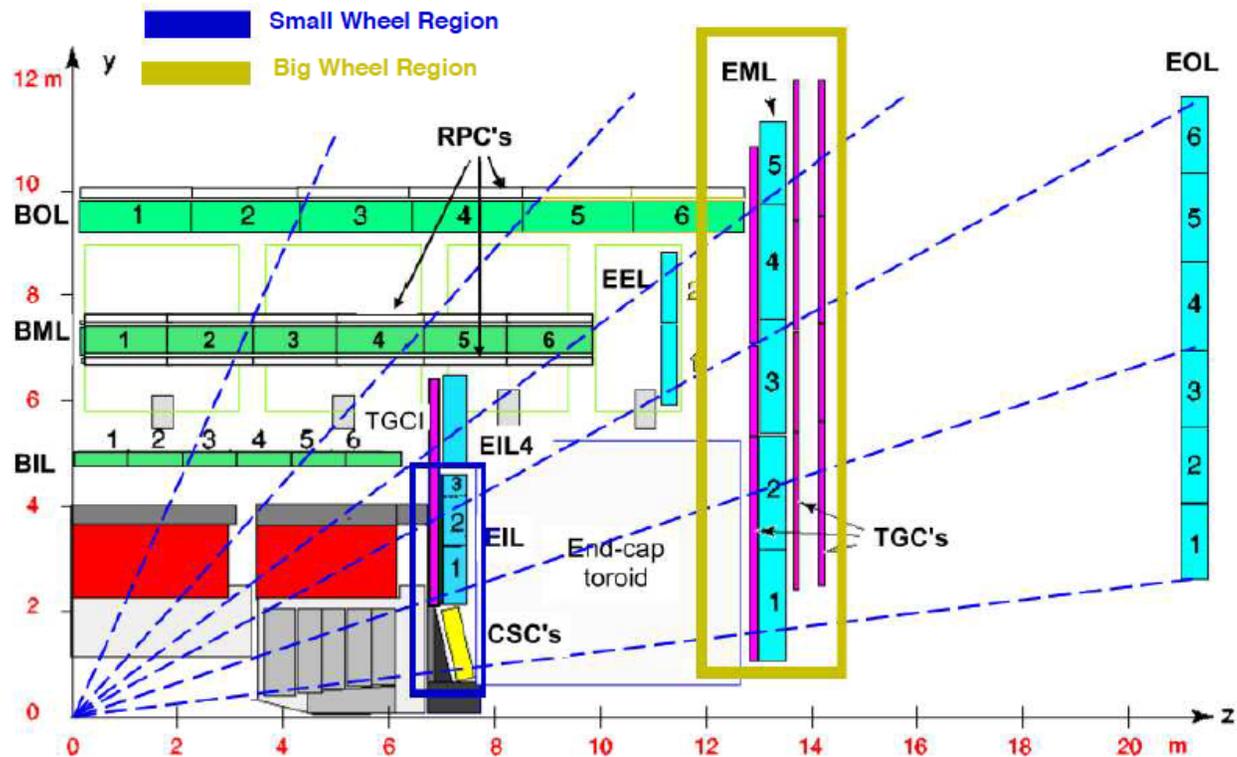


# Readout Architecture in Phase-I Upgrade

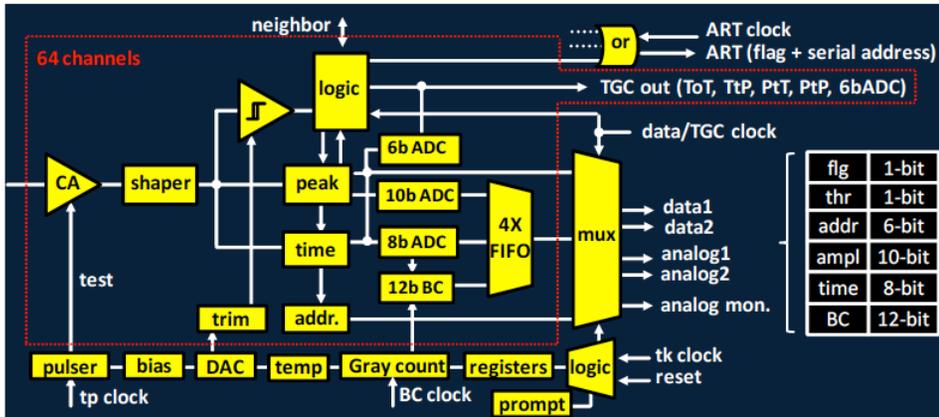


# Muon New Small Wheel

- **Major upgrade in the Muon system to improve trigger rates and reduce false coincidences**
  - new Small Wheel covering  $1.3 < |\eta| < 2.7$  (trigger to  $|\eta| < 2.5$ )
  - replace Cathode Strip Chambers (CSC) with MicroMegas
  - add small-strip Thin Gap Chambers
  - *BNL led the CSC and is contributing to its replacement!*

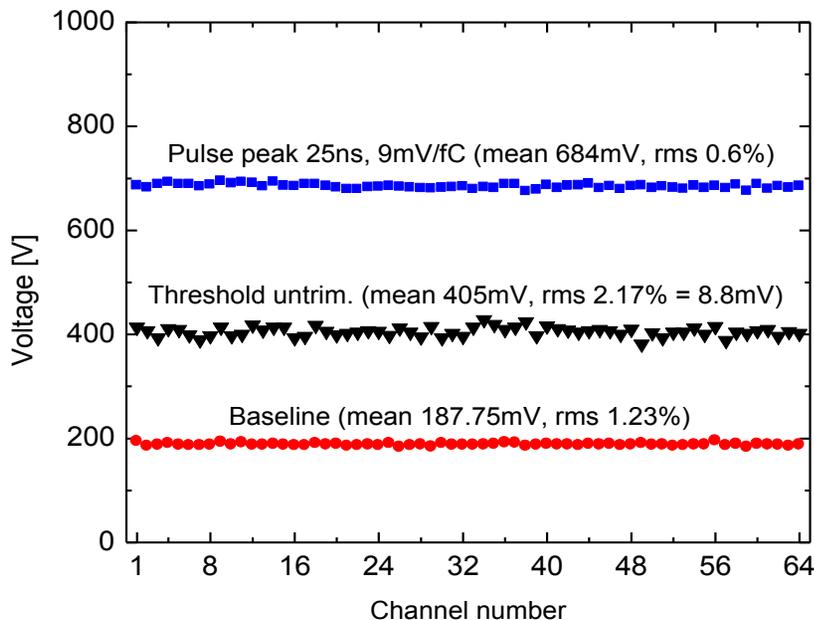


# Front-end ASIC for Muon New Small Wheel (1)



## VMM Chip

- Versatile front-end ASIC for micro-pattern gas detectors
- Suitable to both MicroMegas and sTGC in Muon NSW
- Mixed-signal design, handle both signal polarities
- 64 channels with integrated
  - 10-bit ADC per channel for peak amplitude measurement (multiplexed)
  - 8-bit ADC per channel for sub-nanosecond time measurement (multiplexed)
  - 6-bit FADC (25 ns conversion), 64 channel parallel output for trigger
  - Address of hit channel in real time (Fast OR with address) can also be used in trigger
- Low power, 4-8 mW/channel depending on features used
- CMOS 130 nm, 13.5 x 8.3 mm<sup>2</sup>, over 5 million transistors
- Excellent performance on VMM1 & VMM2, VMM3 development is ongoing

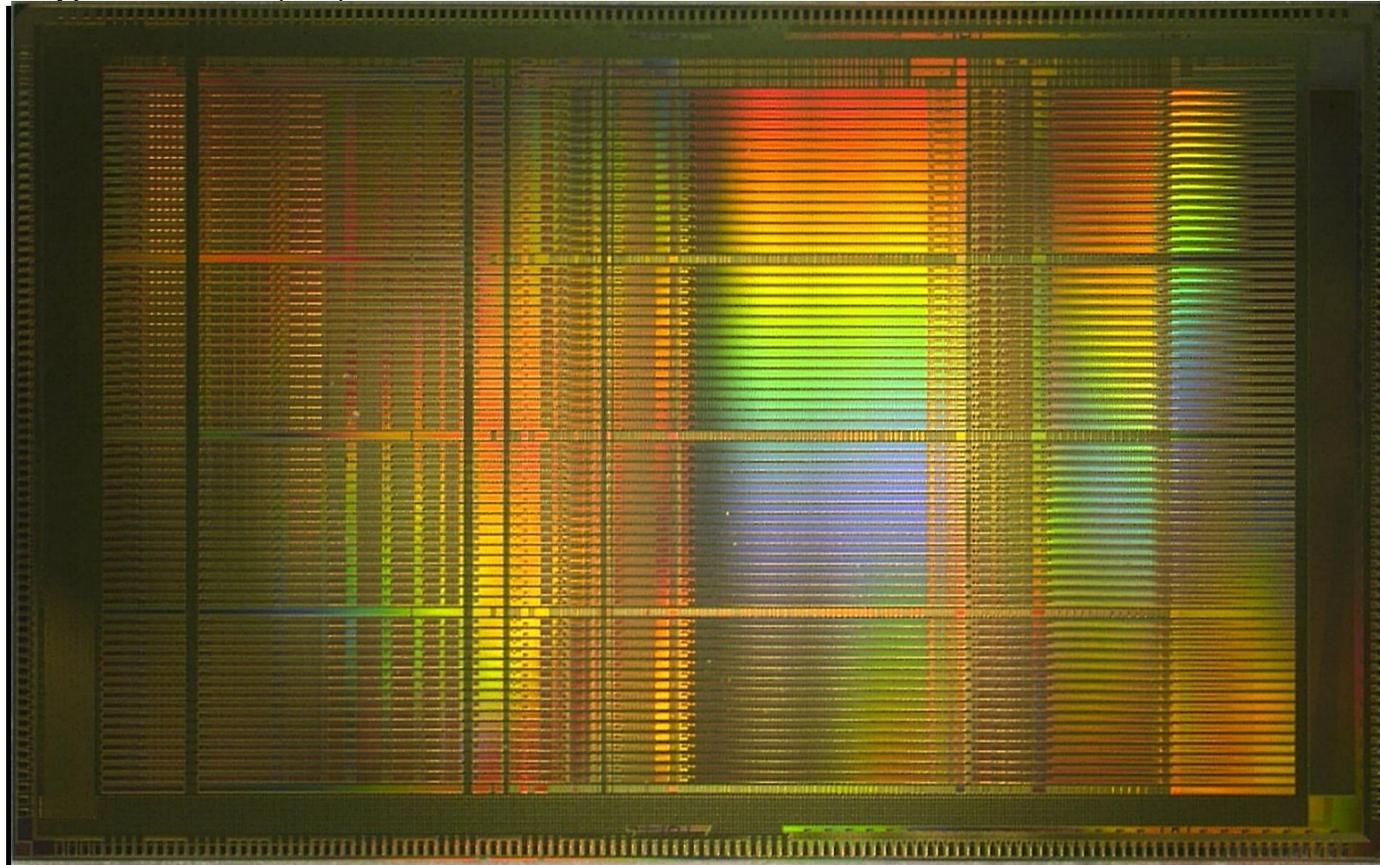


# Front-end ASIC for Muon New Small Wheel (2)

- Layout and Packaging

analog, mixed-signal, digital supplies (1.2V) – neigh.t – digital IOs (14) - TGC outs 0-6

64 inputs, 9 preamplifier supply (1.2V)



TGC outs 7-42

analog, mixed-signal, digital supplies (1.2V) – neigh.b – TGC outs 43-63

13.5 mm **392 bonding pads**

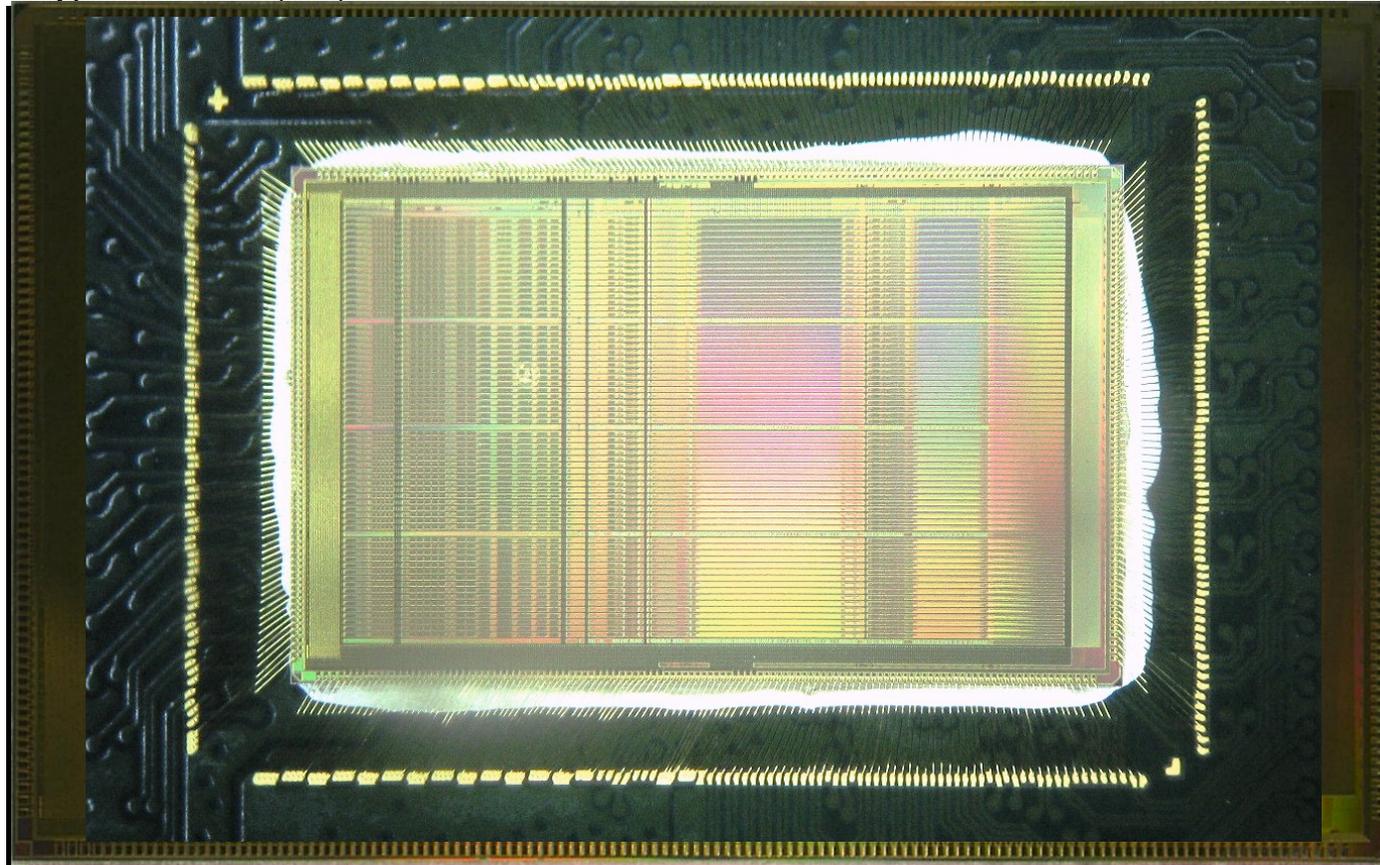
10/06/2015

# Front-end ASIC for Muon New Small Wheel (2)

- Layout and Packaging

analog, mixed-signal, digital supplies (1.2V) – neigh.t – digital IOs (14) - TGC outs 0-6

64 inputs, 9 preamplifier supply (1.2V)



TGC outs 7-42

analog, mixed-signal, digital supplies (1.2V) – neigh.b – TGC outs 43-63

13.5 mm **392 bonding pads**

10/06/2015

# Level 1 Calorimeter Trigger

- **High  $p_T$   $W$ ,  $Z$ , &  $H$  bosons, top quarks, and exotic particles are key part of ATLAS physics program**

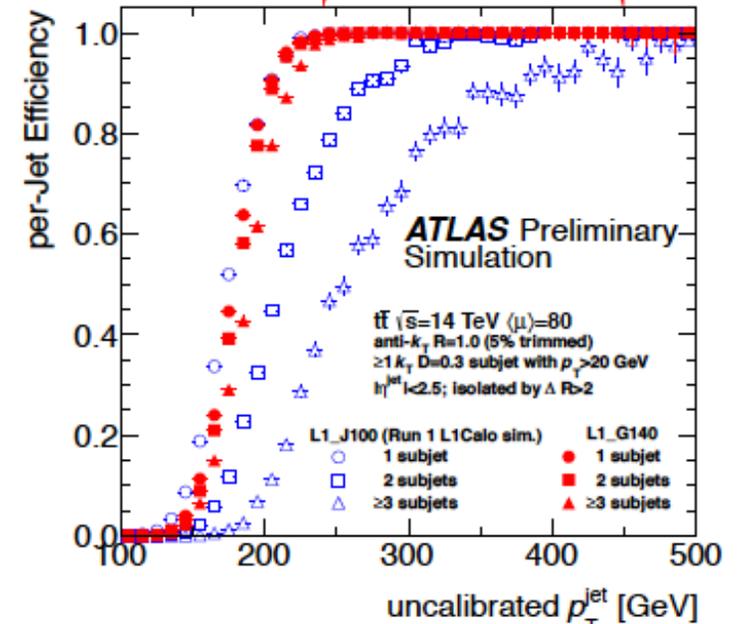
- analyses use jets with  $R = 1.0$  or larger and utilize jet substructure information

- **BNL proposed triggering on large radius jets with entire calorimeter on a single board (gFEX)**

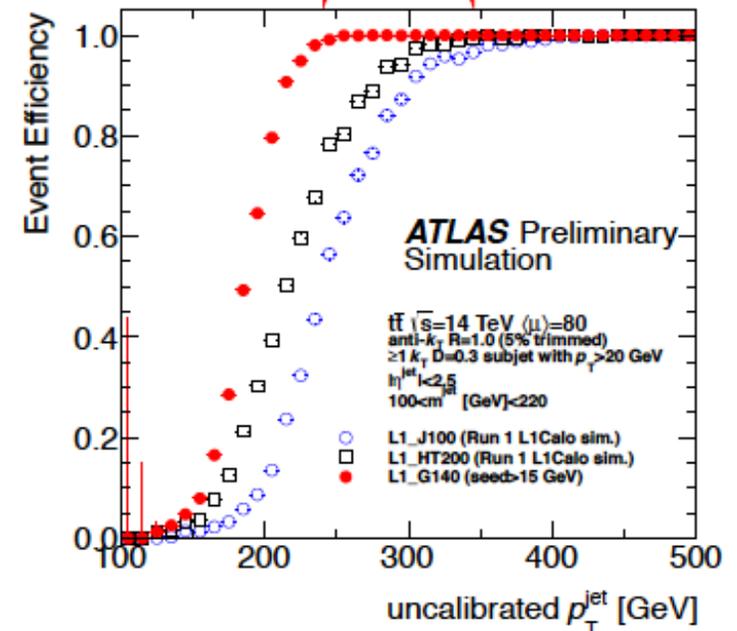
- utilize jet substructure for rejection
- **factor of 2 increase in jet trigger acceptance for boosted  $H \rightarrow b\bar{b}$**
- measures and suppresses pileup contributions  $\Rightarrow$  30% rate reduction for large- $R$  jet triggers
- other use cases being explored
  - $E_T^{\text{miss}}$  with pileup suppression
  - “jets without jets” (Bertolini, Chan, Thaler, hep-ph/1310.7584)
  - event-shape observables
  - centrality-dependent heavy ion variables
- **unique trigger concept developed by BNL**

Synergy between Physics & Performance interests and Detector & Electronics expertise at BNL!

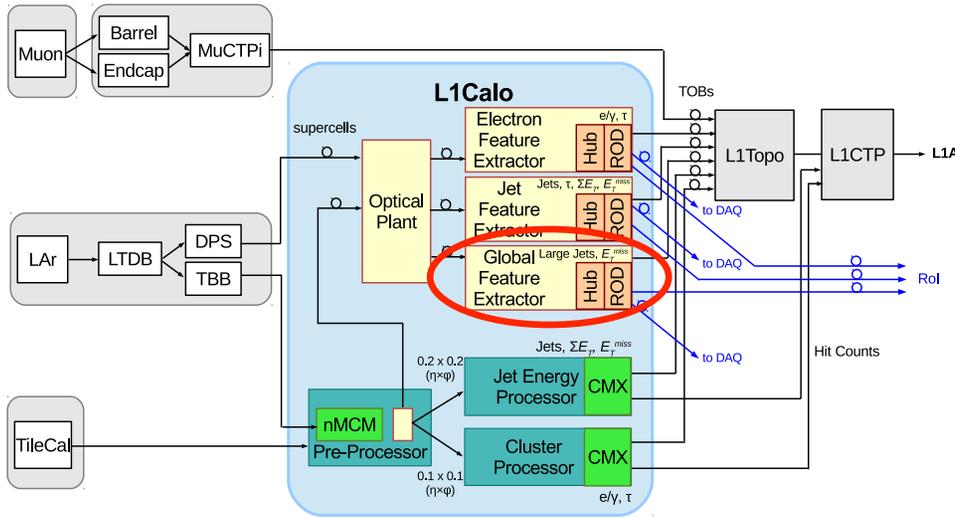
acceptance gain for boosted top



acceptance gain for  $H \rightarrow b\bar{b}$



# Global Feature Extractor in L1Calo (1)



- gFEX is a single ATCA module to process entire ATLAS calorimeter information for large-R jet finding

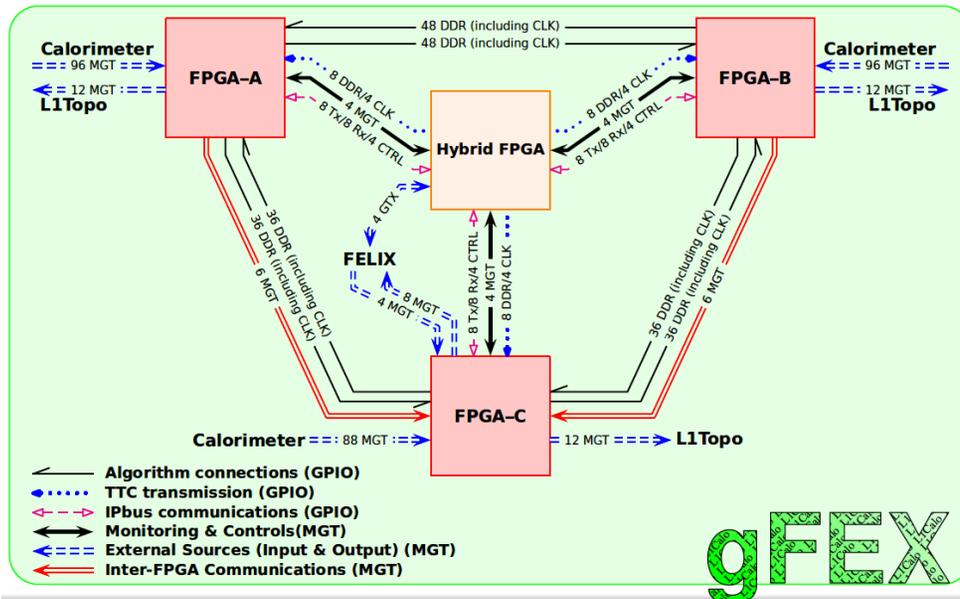
- Strong physics case has been established

- Passed ATLAS preliminary design review at CERN in November 2014

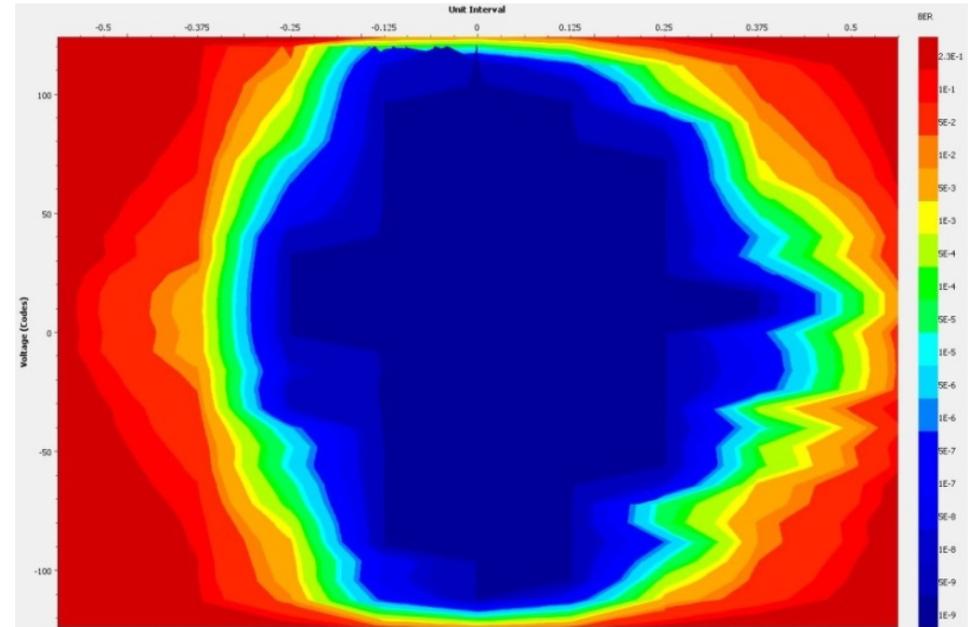
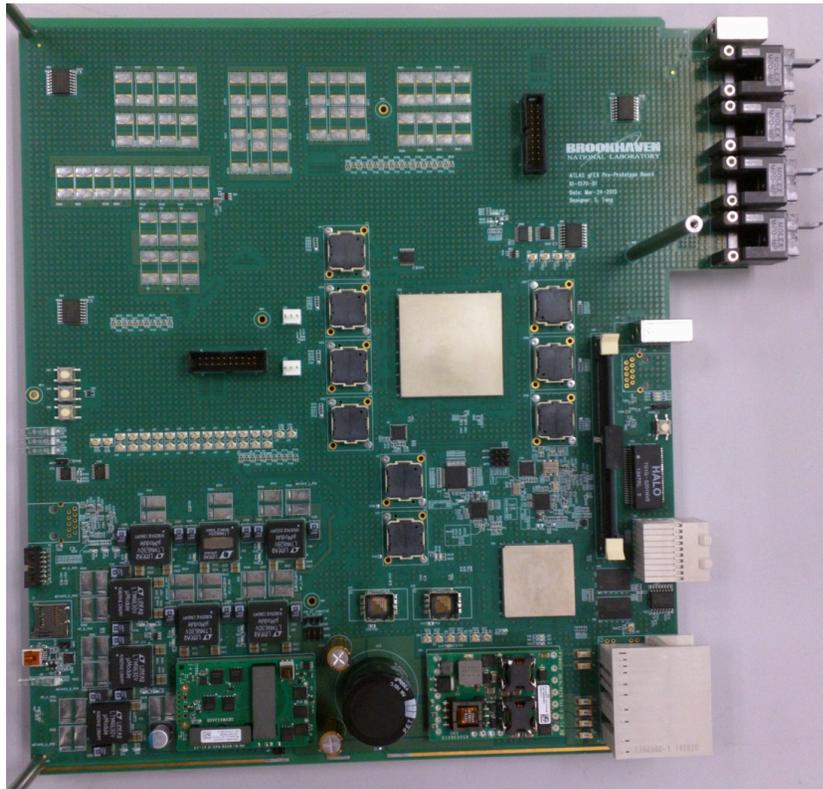
- High density optical I/O – 280 input links from Calorimeters

- High speed optical link – 6.4 Gb/s to 12.8 Gb/s

- Fast data processing in FPGA for jet finding – 5 BCs or 125 ns



# Global Feature Extractor in L1 Calo (2)



Name: SCAN\_19  
Description: MPOD\_X1Y29\_X1Y16\_12.8G  
Started: 2015-Sep-09 14:18:06  
Ended: 2015-Sep-09 14:19:18

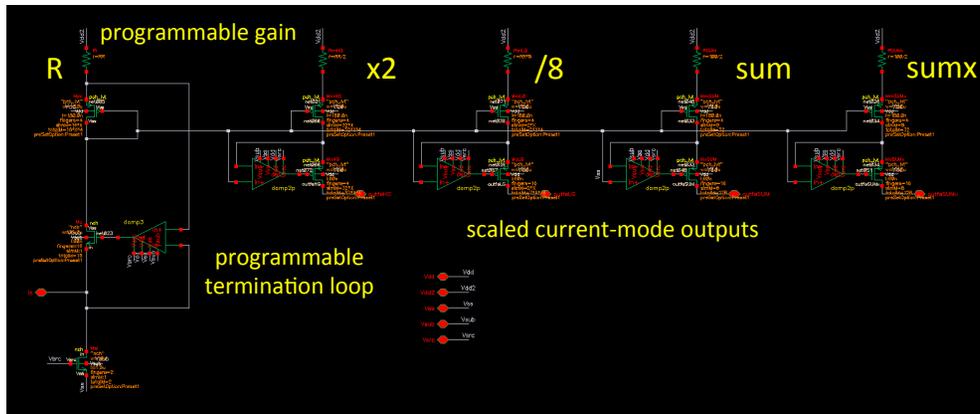
Processor FPGA/MiniPODs link at 12.8 Gb/s  
-3 FPGA with 13.1Gb/s GTH

- Prototype 1
  - 1 Virtex-7 FPGA
  - Zynq SoC
  - Board Infrastructure
  - Test components, interfaces & routing
- Excellent link performance on gFEX Prototype 1
- IBERT at 12.8 Gb/s with  $< 1.2 \times 10^{-15}$  BER with *all 80 Virtex-7 GTH* and *all 16 Zynq GTX* running *simultaneously*

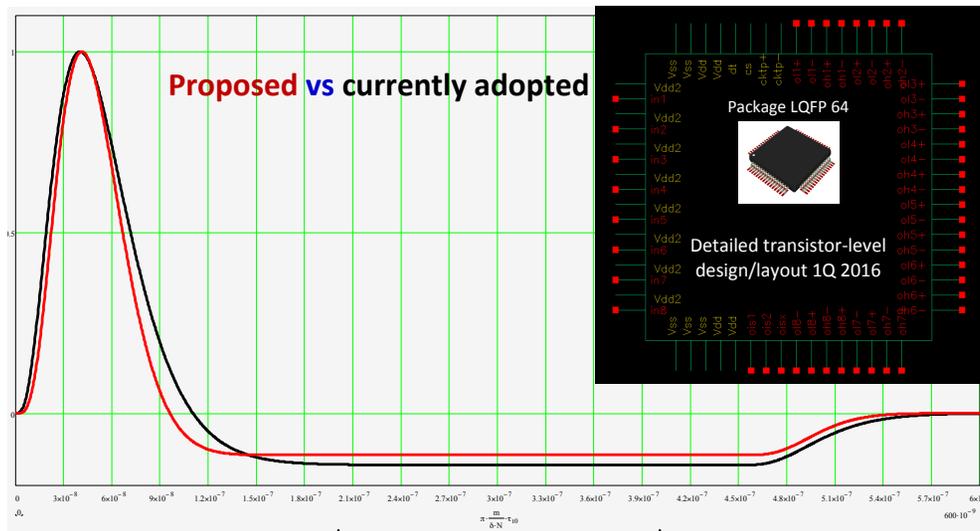
# Motivations for Front-End System-on-Chip (FESOC)

- FESOC will greatly simplify the design of FEB-2
  - Evaluation of FESOC will serve the purpose of prototype development of FEB-2
  - Full solution of FEB-2 will be gradually developed along FESOC development, from board design, power and cooling design, system integration to final production and installation
  - Limited R&D in early FYs is required for FEB-2 design and integration
- The main FEB-2 development will focus on chip level integration instead of board level integration
- FESOC will reduce the power consumption significantly
  - Will ease the system design, including LVPS and cooling
- 65nm CMOS is a potentially viable solution for FESOC
  - Need to demonstrate analog front-end with satisfactory performance
  - A few on-going developments for ADC
  - lpGBTx is being developed in 65nm CMOS at CERN

# R&D of Front-End System-on-Chip (FESOC)

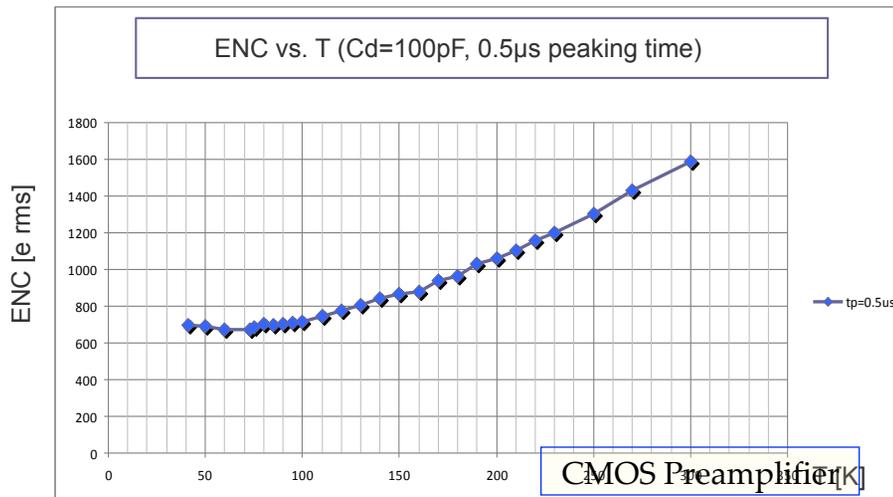
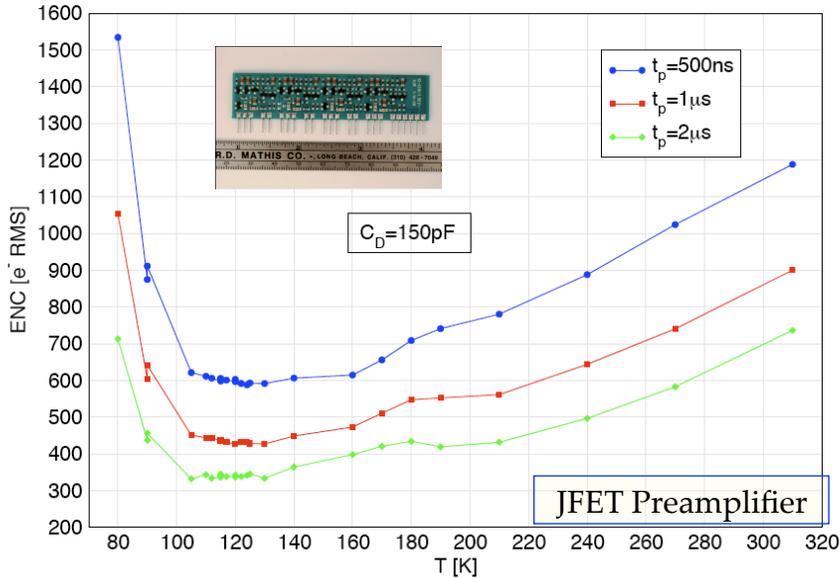


- FESOC will greatly simplify the design of FEB-2
  - The main FEB-2 development will focus on chip level integration
  - FESOC will reduce the power consumption significantly, ease the system power and cooling management
- 65nm CMOS is a potentially viable solution for FESOC
  - Unbalanced differential amplifier with programmable gain/termination, and high-order programmable anti-aliasing filters
  - At equal peaking time offers smaller tail and faster return to baseline, thus lower the pile-up
- Will first demonstrate analog front-end with satisfactory performance
  - Following by the integration of 12-bit/14-bit ADC on chip
  - Final FESOC will use lpGBTx IP core currently being developed at CERN



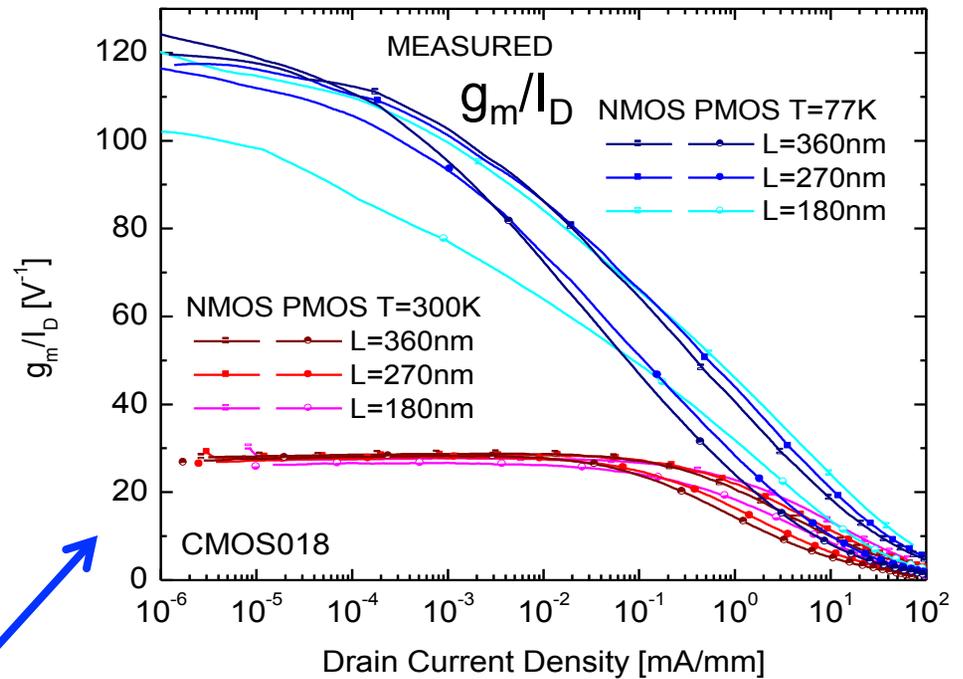
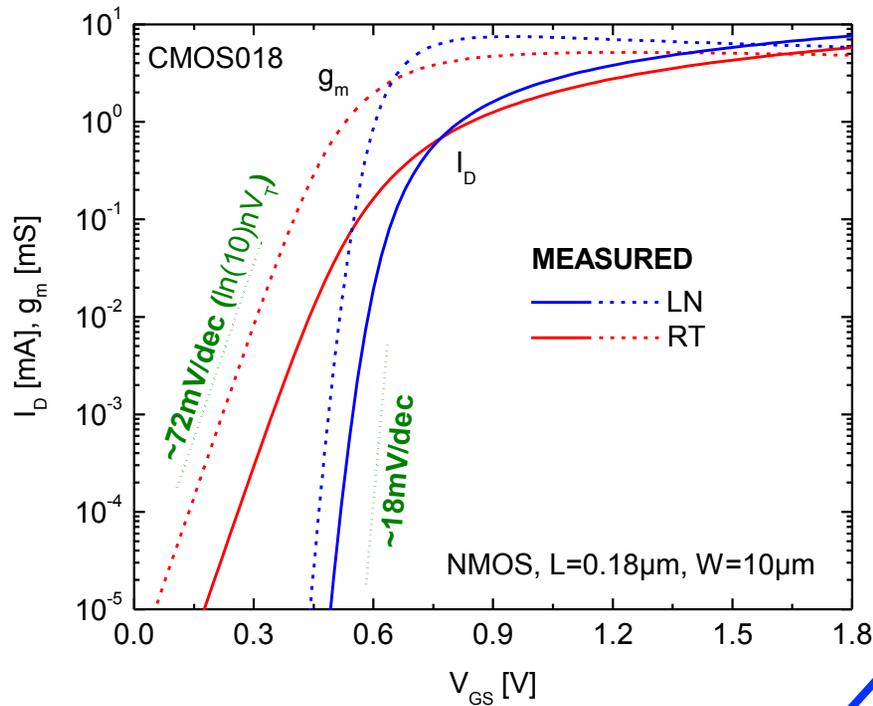
# Cold Electronics: From JFET to CMOS

Equivalent Noise Charge vs. Temperature  
(First Measurements on a Quad-preamplifier prototype)



- BNL has a long history of development of cold electronics
  - NA34/HEILOS, NA48/NA62
- JFET based preamplifier designed for MicroBooNE
  - Bulk mobility and transconductance increase as temperature decreases, carrier freeze out causes ENC increasing when temperature lower than ~100K
- CMOS technology – test result of an existing ASIC in  $0.25 \mu\text{m}$  (*not designed for LAr*)
  - CMOS in LAr has less than half the noise as that at room temperature, higher mobility and higher transconductance/current ratio
- MicroBooNE has adopted the cryogenic CMOS analog front end ASIC developed for DUNE LAr TPC program

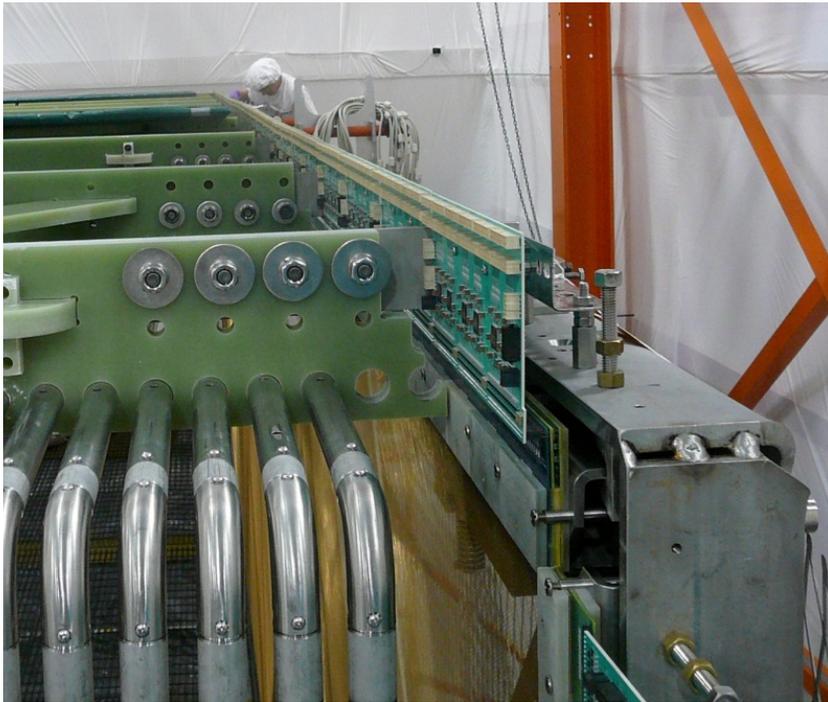
# CMOS Characteristics in LAr



Transconductance/  
drain current  $\rightarrow \frac{g_m}{I_D} \rightarrow \frac{q}{nk_B T} = \begin{cases} \sim 30 & \text{at } T = 300K \\ \sim 116 & \text{at } T = 77K \end{cases}$

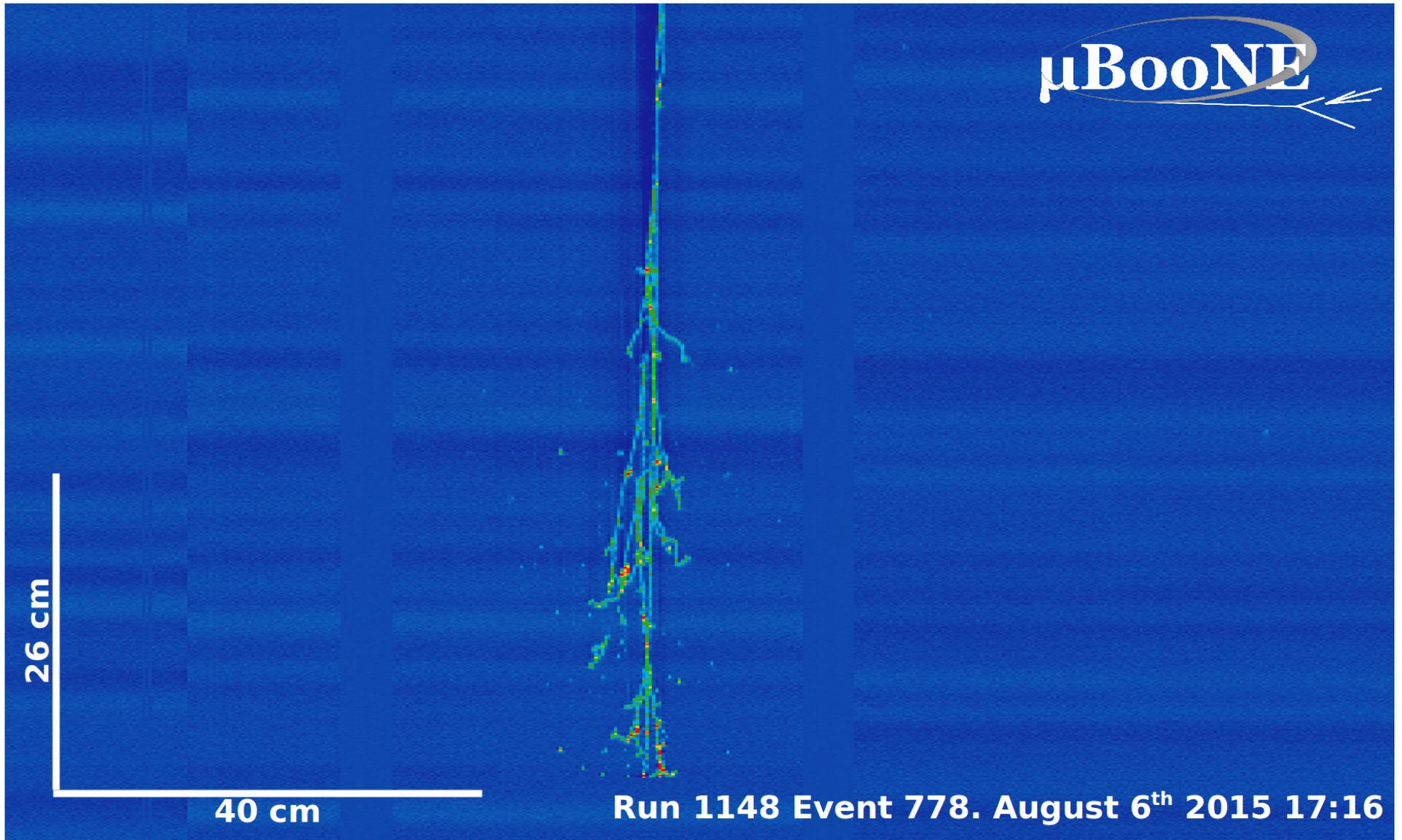
At 77-89K, charge carrier **mobility** in silicon increases and **thermal fluctuations decrease** with  $kT/e$ , resulting in a **higher gain, higher  $g_m/I_D$ , higher speed** and **lower noise**.

# MicroBooNE Front-end Electronics (3)



- **50 cold mother boards (8,256 channels)** are installed on MicroBooNE TPC, all channels tested successfully
- The full chain of front-end readout electronics has been installed in cryostat and tested successfully in January 2014
- Detector has been moved to experimental hall in June 2014

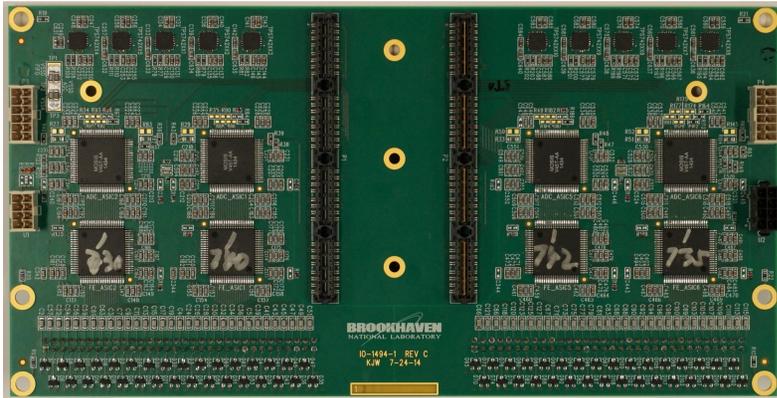
# Cosmic Rays Events in MicroBooNE @ 230V/cm



# SBND/DUNE Front-end Electronics

- Readout chain ASICs are integrated with the TPC electrodes in LAr to minimize the capacitance and noise
- On chip **digitization** to convert to digital signals inside detector cryostat
- **Multiplexing** to high speed serial link, to reduce cable plants, minimize outgassing, make possible the scalability to larger detector volumes
- **Cold FPGA** to house the flexible algorithms for data processing and data reduction
  - An important component for near term project before digital ASIC becomes available
- Industry standard serial link interface to connect directly to back end system minimizing conventional DAQ hardware

# DUNE 35 Ton Cold Electronics – Basis of SBND/DUNE FEMB Design



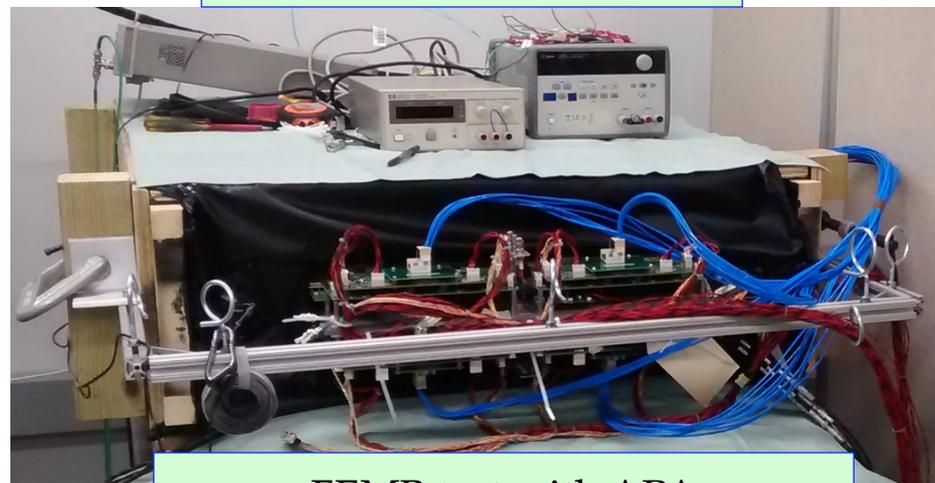
Analog Mother Board



FPGA Mezzanine



Front End Mother Board Assembly



FEMB test with APA

- DUNE 35 ton installation and commissioning is ongoing

# R&D on Cold Electronics

- R&D of CMOS cold electronics started in 2008
  - Analog FE ASIC was the first one developed, following by ADC ASIC development, studies of cold regulator and FPGA etc.
  - In parallel, studies of CMOS lifetime and reliability at 77 K were conducted
    - *"LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Trans. on NSci, 60, No: 6, Part: 2, p4737(2013)*
  - Gradually build up a full solution of cold front end readout electronics chain
- Projects using, and potentially will be using cold electronics:
  - MicroBooNE
  - ARGONTUBE
  - LArIAT
  - SBND
  - ICARUS 50l TPC at CERN
  - DUNE 35Ton
  - ProtoDUNE at CERN
  - DUNE 10kt Far Detector
- *R&D on cold electronics started before most of these projects were anticipated or in existence → an example of long term R&D with high impact*

# Collaboration With Universities

- *P5 Recommendation 28: Strengthen university-national laboratory partnerships in instrumentation R&D through investment in instrumentation at universities. Encourage graduate programs with a focus on instrumentation education at HEP supported universities and labs, and fully exploit the unique capabilities and facilities offered at each.*
- Collaboration universities
  - ATLAS detector upgrade
    - Arizona, Chicago, Columbia, Harvard, Indiana, Penn, Pittsburgh, SMU, Stony Brook, UT Dallas, Yale
  - Neutrino experiments
    - Chicago, Cincinnati, Columbia, MSU, Penn, SMU, Syracuse, Yale